

# **JEDEC STANDARD**

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## **PMIC5200 Power Management IC Standard**

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### **JESD301-3**

**Version 1.0**

**October 2025**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## PMIC5200 Power Management IC Standard

(From JEDEC Board Ballot JCB-25-49, formulated under the cognizance of the JC-40.1 subcommittee on Digital Logic Families and Applications, item 159.10B).

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### 1 Scope

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This standard defines the specification of interface parameters, signaling protocols, and features for PMIC devices used for memory module applications. The designation PMIC5200 refers to the device specified by this document.

The purpose is to provide a standard for the PMIC5200 device for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

Unless otherwise noted in the document, any illegal operation is not allowed, and device operation is not guaranteed.

NOTE: The designation PMIC5200 refers to a portion of the part number designation of a series of commercial logic devices common in the industry. This number is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

#### 1.1 Description

The PMIC5200 is designed for typical LPDDR5 CAMM2. The PMIC features four step down switching regulators and two LDO regulators.

The PMIC is designed to support approximately TBD Watts of power. The PMIC is powered from VIN\_Bulk input for the entire PMIC including the switching regulators and LDO output regulators. The PMIC supports selectable interface (I<sup>2</sup>C or I<sup>3</sup>C Basic) to fit various application environment. The PMIC device is intended to operate up to 12.5 MHz on a 1.0 V I<sup>3</sup>C Basic bus or up to 1 MHz on 1.0 V to 3.3 V I<sup>2</sup>C bus.

## 1.2 Feature Summary

**Table 1 — PMIC5200 - Current Capability**

Device	SWA	SWB	SWC	SWD	Unit
PMIC5200 - Current Capability per Phase	7.5	1.2	1.0	1.2	A

- VIN\_Bulk input supply range: 3.0 V to 5.5 V
- Four step down switching regulators: SWA, SWB, SWC and SWD
- 2 LDO regulators: VOUT\_1.8V, VOUT\_1.0V
- Error injection capability
- Persistent error log registers
- Secure mode and programmable mode of operation
- Independently programmable output voltages, power up and power down sequence for switch regulators
- Output power good status reporting mechanism
- VIN\_Bulk input supply protection feature: Input over voltage
- Output switch regulators protection features: Output over voltage, output under voltage, output current limiter
- Output current and power measurement, output current threshold mechanism
- Temperature measurement, temperature warning threshold, critical temperature shutdown
- Multi Time Programmable (MTP) Non-Volatile Memory
- Programmable and CAMM2 specific registers for customization
- Flexible Open Drain IO (I<sup>2</sup>C) and Push Pull (I3C Basic) IO support
- Flexible mechanism to enable switch regulators (w/ VR\_EN pin or VR Enable command on I<sup>2</sup>C or I3C Basic interface or Auto Power On)
- Quiescent Power State (P1 State)
- Dynamic Voltage Frequency Scaling VDDQ (DVFSQ) function for SWB with DVFSQ\_n pin
- Unlock pin for unlocked, locked and configurable lock operation
- SWB Disable Override function
- PMIC warranty status bit
- Fine resolution ADC (31.25 mA/mW step size)

## 2 Package

### 2.1 Package Pinout

The PMIC device is packaged in 5 mm x 5 mm FCQFN. The PMIC pinout is shown in [Figure 1](#) and [Figure 2](#) for Top view and Bottom view, respectively.

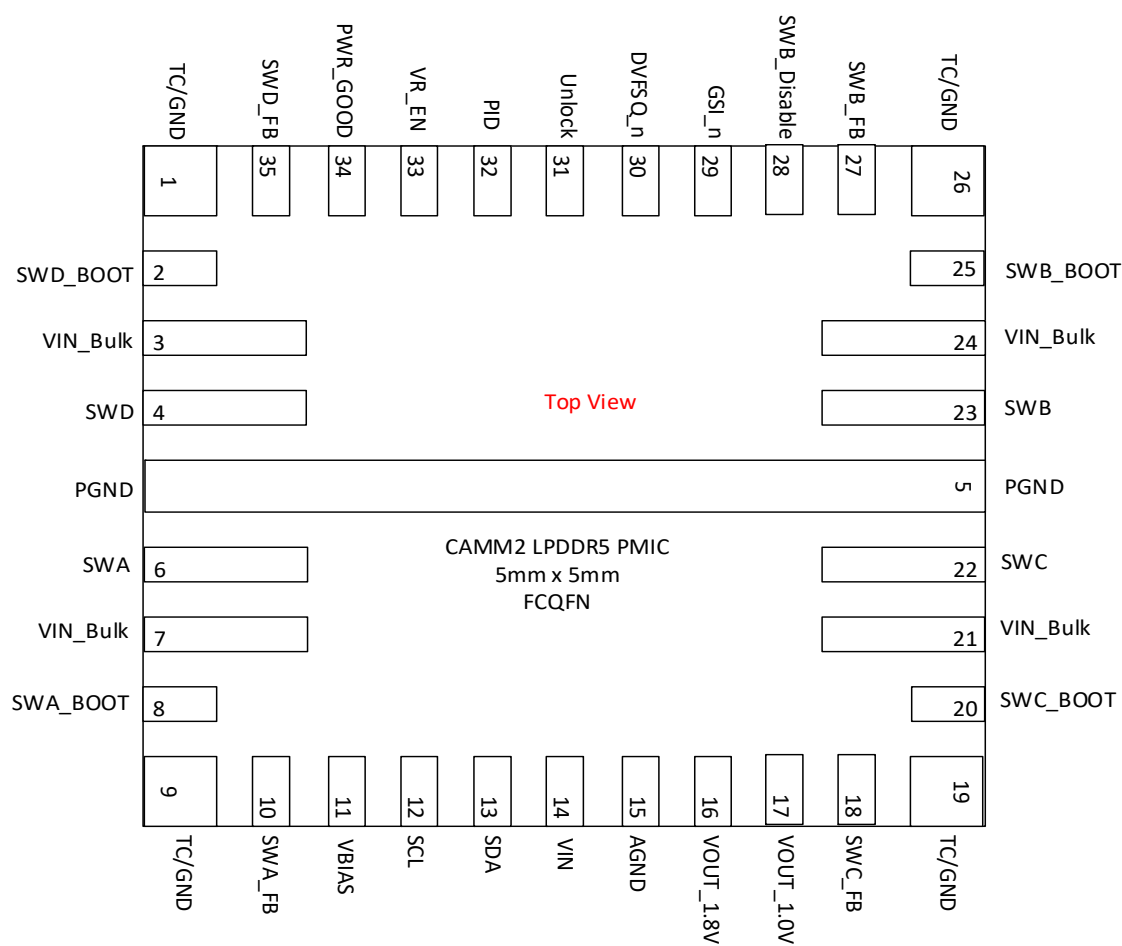


Figure 1 — PMIC Package - Top View

## 2.1 Package Pinout (cont'd)

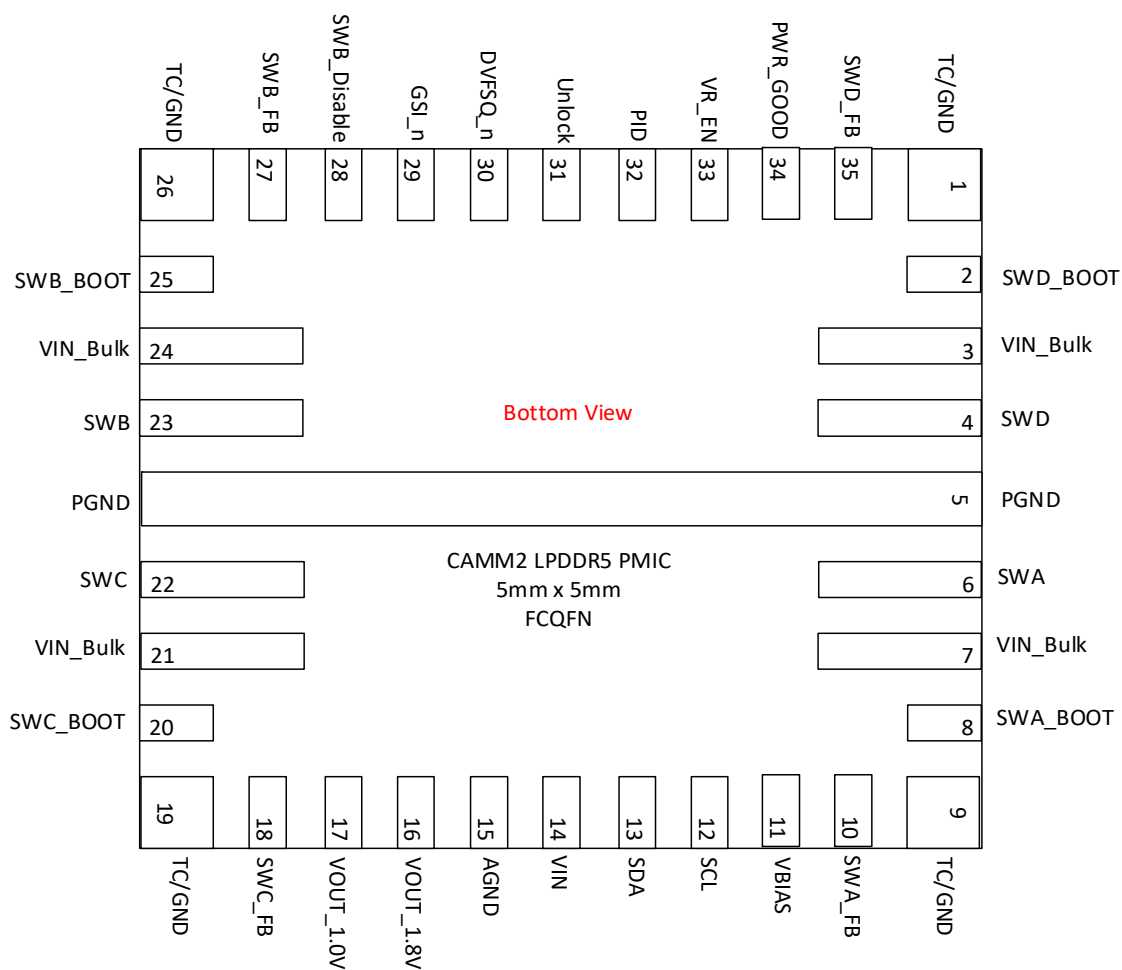


Figure 2 — PMIC Package - Bottom View

## 2.2 Pin List

**Table 2 — PMIC Pin Description**

Pin Name	Type	Description
VIN_Bulk (4x)	I	5 V power input supply pin to the PMIC. All four VIN_Bulk input pins must be connected to the 5V input supply even if one or more output regulators are not intended to be used.
VIN	I	5 V power input supply pin to the PMIC for analog circuits.
PWR_GOOD	IO	Power good indicator. Open drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceeds the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin transitions from high to low. The LDO outputs shall remain on.
VBias	PWR	Vbias Voltage generated by PMIC.
SCL	I	I <sup>2</sup> C/I <sup>3</sup> C Basic Clock Input for management bus.
SDA	IO	I <sup>2</sup> C/I <sup>3</sup> C Basic Data Input/Output for management bus.
SWA	O	Output switch node A buck regulator. This pin connects to L1 power inductor. The SWA output must not be connected to SWB output even if they are configured as same exact output voltage.
SWA_BOOT	PWR	Bootstrap node for SWA high side NMOS driver. This pin connects to SWA through a high quality capacitor.
SWA_FB	I	This pin connects to CAMM2 power plane load.
SWB	O	Output switch node B buck regulator. This pin connects to L2 power inductor. The SWB output must not be connected to SWA output even if they are configured as same exact output voltage.
SWB_BOOT	PWR	Bootstrap node for SWB high side NMOS driver. This pin connects to SWB through a high quality capacitor.
SWB_FB	I	This pin connects to CAMM2 power plane load.
SWC	O	Output switch node C buck regulator. This pin connects to L3 power inductor.
SWC_BOOT	PWR	Bootstrap node for SWC high NMOS driver. This pin connects to SWC through a high quality capacitor.
SWC_FB	I	This pin connects to CAMM2 power plane load.
SWD	O	Output switch node D buck regulator. This pin connects to L4 power inductor.
SWD_BOOT	PWR	Bootstrap node for SWD high side NMOS driver. This pin connects to SWD through a high quality capacitor.
SWD_FB	I	This pin connects to CAMM2 power plane load.
PID	I	PMIC ID pin for I <sup>2</sup> C and I <sup>3</sup> C Basic bus. This pin connects to CAMM2 ground plane or VOUT_1.8V rail or left floating.
VOUT_1.8V	O	1.8V LDO Output.
VOUT_1.0V	O	1.0 V LDO Output.
AGND	PWR	Analog Ground. Connects to CAMM2 ground plane.
PGND	PWR	Power Ground. Connects to CAMM2 ground plane.

**Table 2 — PMIC Pin Description (cont'd)**

Pin Name	Type	Description
VR_EN	I	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
SWB_Disable	I	<p>If SWB_Disable input pin function is enabled, the PMIC keeps the SWB output regulator disabled when the SWB_Disable input pin is high at the time of VR Enable command.</p> <p>If SWB_Disable input pin function is enabled, the PMIC follows the normal power on sequence config 0 to power on sequence config 3 registers when the SWB_Disable input pin is low at the time of VR Enable command.</p> <p>If SWB_Disable input pin is disabled, the PMIC input receiver is off and PMIC follows the normal power on sequence config0 to config3 registers.</p> <p>On the CAMM2 PCB, this pin has an external 100KΩ pulldown resistor to GND. This pin shall not be left floating.</p>
TC/GND		Thermal connection to GND. This pin is connected to GND on the PCB and may or may not be connected to GND on the die.
Unlock	I	<p>Active High Asynchronous input.</p> <p>If Unlock pin function is enabled, register R2F[2] value follows the Unlock input pin level. When this input pin is high, it updates R2F[2] to '1' and puts PMIC in a programmable mode; when this input pin is low, it updates R2F[2] to '0' and puts PMIC in a secure mode.</p> <p>If Unlock pin function is disabled, the input receiver is disabled and this pin has no effect on PMIC. The register R2F[2] definition applies for secure and programmable mode operation.</p>
DVFSQ_n	I	<p>Active Low Asynchronous input. Edge triggered, Active low.</p> <p>If DVFSQ_n pin function is enabled, when this input pin transitions from high to low while in the P3 state, the PMIC enters DVFSQ state where the PMIC SWB output voltage is as defined in register R3E[7:1] and R2B [3] at slew rate defined in R2E[7:6]. When this input pin transitions from low to high while in DVFSQ state, the PMIC SWB output voltage is as defined in register R25[7:1] and R2B[3] at slew rate defined in R2E[7:6].</p> <p>If DVFSQ_n pin is disabled, the input receiver is disabled and this pin has no effect on SWB output voltage, and entry into the DVFSQ power state is disabled.</p>
GSI_n	O	General Status Interrupt; Open Drain Output. When this pin is enabled, the PMIC asserts this pin low to communicate any one or more events to host. This pin stays asserted until the appropriate registers are explicitly cleared and the event is no longer present.

### 3 Electrical Specifications

#### 3.1 Input Supply and Output Regulator Electrical Characteristics

##### 3.1.1 Input Supply Electrical Characteristics

Table 3 — Input Supply DC + AC Specification<sup>[1]</sup>

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bulk Input Supply Voltage	VIN_Bulk	3.0	5.0	5.5	V	[2]
Bulk Input Supply Maximum AC Voltage	VIN_Bulk_AC	-	-	6.5	V	
Maximum voltage on VIN_Bulk during soft stop	VIN_Bulk_Soft_Stop_Max	-	-	5.55	V	[3],[4]
Bulk Input Supply Voltage Ramp Up Rate	VIN_Bulk_Ramp_Up	0.01	-	3.0	V/ms	[5]
Bulk Input Supply Voltage Ramp Down Rate	VIN_Bulk_Ramp_Down	0.01	-	1.0	V/ms	[6]
Bulk Input Supply Voltage Start Up Overshoot	VIN_Bulk_OS_STARTUP	-	-	TBD	V*μs	[7]
VIN_Bulk Input Supply Current	I <sub>VIN_Bulk</sub>	0.05	-	2.0	A	[8]
	I <sub>VIN_Bulk_5.0V</sub>	5.2	-	7.5	A	[9]
	I <sub>VIN_Bulk_3.3V</sub>	7.8	-	9.5	A	[9]
VIN_Bulk Input Supply Quiescent Current	I <sub>VIN_Bulk_Quiescent</sub>	-	-	25	μA	[10]
VIN_Bulk Input Supply Idle Current	I <sub>VIN_Bulk_Idle</sub>	-	-	TBD	μA	[11]

NOTE 1 Input supply is referred in this table are VIN\_Bulk and VIN.

NOTE 2 During first power on, the input voltage supply must reach a minimum 3.0 V for PMIC to detect valid input supply.

NOTE 3 The maximum VIN\_Bulk input supply voltage rise during soft stop for SWx soft stop operation.

NOTE 4 The maximum VIN\_Bulk input supply voltage rise is tested with VIN\_Bulk = 5.5 V, SWA = 1.05 V, SWB = 0.5 V, SWC = 1.8 V and SWD = 0.9 V and using the recommended setting from the “LPDDR5/5X PMIC5200 Register Setting for the Soft Stop” table in JESD318. The test condition assumes input VIN\_Bulk supply is not capable of sinking current. The maximum VIN\_Bulk input supply voltage rise is tested with module VIN\_Bulk and output rail decoupling from the “LPDDR5/5X Decoupling guidelines” table in JESD318 and with bulk output capacitance for SWx listed in Section 6.1. This specification defines the DC component of the voltage during soft stop. AC noise that is less than 1μs can be ignored when testing against this spec. The maximum voltage rise is measured under 1MHz bandwidth limiting during soft stop shut down.

NOTE 5 The ramp up rate between 300 mV and 3.0 V.

NOTE 6 The ramp down rate between 3.0 V and 300 mV.

NOTE 7 The area under the curve above VIN\_Bulk = TBD V. VIN\_Bulk\_AC spec must also be satisfied.

NOTE 8 The minimum input current requirement is to deliver the maximum rated output current on VOUT\_1.8V, VOUT\_1.0V LDO plus the current required by the PMIC for its own use. The maximum input current is what PMIC may see on its all VIN\_Bulk input.

NOTE 9 The minimum input current requirement is to deliver the maximum rated output current on VOUT\_1.8V, VOUT\_1.0V LDO, all switch regulator outputs plus the current required by the PMIC for its own use. The maximum input current is what PMIC may see on its all VIN\_Bulk input.

NOTE 10 VIN\_Bulk = 5.0V. Measured at room temperature. All circuitry including output regulators and LDOs are off. VR\_EN signal is static Low or High; I<sup>2</sup>C or I<sup>3</sup>C Basic interface access is not allowed and bus is pulled High. PID signal is pulled either High or Low.

NOTE 11 VIN\_Bulk = 5.0 V. Measured at room temperature. All output regulators and LDOs are on with 0A output load. VR\_EN signal is static Low or High. I<sup>2</sup>C or I<sup>3</sup>C Basic interface access is allowed and bus is pulled High. PID signal is pulled either High or Low.

### 3.1.2 Switch Regulator Output Electrical Characteristics

**Table 4 — SWA - Single Phase Regulator; DC + AC Specification**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.05		V	[1]
Maximum Continuous DC Current Load	Itdc	0	-	7.5	A	[2]
Maximum Peak Instantaneous Current	Ipeakmax	-	-	11.5	A	[3]
Maximum Load Transient	dI/dt	-	-	10	A/μs	[4]
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	[5],[6]
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	[7]

NOTE 1 Typical voltage configured in the register Table 137, "Register 0x21," [7:1].

NOTE 2 Measured over long period of time. Typically 1 second.

NOTE 3 Measured over short period of time. Typically  $\geq 20 \mu\text{s}$  but less than  $50 \mu\text{s}$ .

NOTE 4 This parameter is applied to measure output voltage regulator DC+AC tolerance.

NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN\_Bulk can vary from minimum to maximum value specified in Table 3, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN\_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load Itdc = 0 A.

**Table 5 — SWD - Single Phase Regulator; DC + AC Specification**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		0.9		V	[1]
Maximum Continuous DC Current Load	Itdc	0	-	1.2	A	[2]
Maximum Peak Instantaneous Current	Ipeakmax	-	-	2	A	[3]
Maximum Load Transient	dI/dt	-	-	2	A/μs	[4]
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	[5],[6]
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	[7]

NOTE 1 Typical voltage configured in the register Table 139, "Register 0x23," [7:1].

NOTE 2 Measured over long period of time. Typically 1 second.

NOTE 3 Measured over short period of time. Typically  $\geq 20 \mu\text{s}$  but less than  $50 \mu\text{s}$ .

NOTE 4 This parameter is applied for the measurement of the output voltage regulator accuracy.

NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN\_Bulk can vary from minimum to maximum value specified in Table 3, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN\_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load Itdc = 0 A.



### 3.1.2 Switch Regulator Output Electrical Characteristics (cont'd)

**Table 6 — SWB - Single Phase Regulator; DC + AC Specification**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		0.5		V	[1]
Maximum Continuous DC Current Load	Itdc	0	-	1.2	A	[2]
Maximum Peak Instantaneous Current	Ipeakmax	-	-	2	A	[3]
Maximum Load Transient	dI/dt	-	-	2	A/μs	[4]
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	[5],[6]
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	[7]

NOTE 1 Typical voltage configured in the register Table 141, "Register 0x25," [7:1].

NOTE 2 Measured over long period of time. Typically 1 second.

NOTE 3 Measured over short period of time. Typically  $\geq 20 \mu\text{s}$  but less than  $50 \mu\text{s}$ .

NOTE 4 This parameter is applied to measure output voltage regulator DC+AC tolerance.

NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN\_Bulk can vary from minimum to maximum value specified in Table 3, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN\_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load Itdc = 0 A.

**Table 7 — SWC - Single Phase Regulator; DC + AC Specification**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output Voltage	Vout		1.8		V	[1]
Maximum Continuous DC Current Load	Itdc	0	-	1	A	[2]
Maximum Peak Instantaneous Current	Ipeakmax	-	-	2	A	[3]
Maximum Load Transient	dI/dt	-	-	2	A/μs	[4]
Regulator Output DC + AC Voltage Tolerance	Reg_DC_AC_Tol	-2.5		2.5	%	[5],[6]
Regulator Feedback Set Point Accuracy	FB_Set_Point	-0.75		0.75	%	[7]

NOTE 1 Typical voltage configured in the register Table 143, "Register 0x27," [7:1].

NOTE 2 Measured over long period of time. Typically 1 second.

NOTE 3 Measured over short period of time. Typically  $\geq 20 \mu\text{s}$  but less than  $50 \mu\text{s}$ .

NOTE 4 This parameter is applied to measure output voltage regulator DC+AC tolerance.

NOTE 5 The percentage applies to typical voltage configured in the register. The PMIC bulk input supply voltage VIN\_Bulk can vary from minimum to maximum value specified in Table 3, "Input Supply DC + AC Specification". The regulator output current load can vary maximum dI/dt value. The output ripple is inclusive in this parameter.

NOTE 6 Applies across entire PMIC operating temperature range.

NOTE 7 The percentage applies to typical voltage configured in the register and at a given temperature within operating temperature range. The PMIC bulk input supply voltage VIN\_Bulk is fixed at nominal voltage of 5.0V. The regulator output current load Itdc = 0 A.

### 3.1.3 LDO Output Regulator Characteristics

**Table 8 — LDO Output Regulator DC + AC Specification**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
1.8 V LDO Output Voltage	VOUT_1.8V		1.8		V	[1]
1.8 V LDO Output - Maximum Output Current	I <sub>tdc_VOUT_1.8V</sub>	-	-	25	mA	[2]
1.0 V LDO Output Voltage	VOUT_1.0V		1.0		V	[3]
1.0 V LDO Output - Maximum Output Current	I <sub>tdc_VOUT_1.0V</sub>	-	-	20	mA	[4]

NOTE 1 Typical voltage is configured in register Table 147, "Register 0x2B," [7:6]. The min and max values are guaranteed to be within  $\pm 100$  mV of programmed value.

NOTE 2 The maximum output current represents the external load only and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.8V LDO Power Good status is good (i.e.,  $t_{1.8V\_Ready}$  timing parameter is satisfied). Prior to PMIC's 1.8V LDO Power Good Status (i.e., while PMIC is still ramping up the 1.8V LDO), the maximum output current shall be limited to maximum of 10 mA.

NOTE 3 Typical voltage is configured in register Table 147, "Register 0x2B," [2:1]. The min and max values are guaranteed to be within  $\pm 50$  mV of programmed value.

NOTE 4 The maximum output current represents the external load only and excludes PMIC's own internal current consumption. The specified maximum output current is only applicable after PMIC's 1.0V LDO Power Good status is good (i.e.,  $t_{1.0V\_Ready}$  timing parameter is satisfied). Prior to PMIC's 1.0V LDO Power Good Status (i.e., while PMIC is still ramping up the 1.0V LDO), the maximum output current shall be limited to maximum of 5 mA.

## 3.2 Efficiency

The PMIC5200 efficiency spec is defined for the reference test board only and it is not applicable for any CAMM2 application board which varies from the reference test board. The reference test board includes the inductor and the PCB characteristics which complies with the footnote 1 in [Table 9/Table 10](#). The efficiency spec is only measured for one switch regulator at a time; all other switch regulators must be disabled. The PMIC switching frequency must comply with the footnote 9 in [Table 9/Table 10](#). The typical CAMM2 application environment which deviates from the reference test board, all buck regulators are turned on simultaneously, carries external load on LDOs and signal interface pins may not be held static will have lower efficiency than defined in [Table 9/Table 10](#). The combination of all variation for application environment is not subject to the efficiency spec as defined in [Table 9/Table 10](#).

### 3.2.1 VIN\_Bulk = 5.0 V

**Table 9 — Efficiency Characteristics; VIN\_Bulk = 5.0V<sup>[1]</sup>**

Switch Node Output	Efficiency (% of Max Itdc Load)						Unit	Notes
	15%	20%	25%	50%	75%	100%		
SWA	≥ 85	≥ 86	≥ 86	≥ 88	≥ 84	≥ 82	%	[2],[3],[4],[5],[6],[7],[8],[9],[10],[11]
SWD	≥ 84	≥ 86	≥ 87	≥ 87	≥ 87	≥ 85	%	
SWB; Vout = 0.5V	≥ 77	≥ 79	≥ 80	≥ 84	≥ 82	≥ 79	%	
SWB; Vout = 0.3V	≥ 68	≥ 70	≥ 73	≥ 79	≥ 77	≥ 74	%	
SWC	≥ 86	≥ 88	≥ 90	≥ 89	≥ 87	≥ 85	%	

NOTE 1 The efficiency numbers assume the inductor specification as noted in Section 7.2.

NOTE 2 The maximum Itdc as specified in [Table 4](#) to [Table 7](#) appropriately.

NOTE 3 When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.

NOTE 4 No external load on VOUT\_1.8V, VOUT\_1.0V LDO is applied.

NOTE 5 I<sup>2</sup>C/I<sup>3</sup>C Basic bus is pulled High and held static. PWR\_GOOD signal is pulled High and held static.

NOTE 6 The efficiency includes the buck regulator loss, the PCB loss ( $\leq 2.5 \text{ m}\Omega$  from the SWx output pin of the PMIC to VOUTx bulk capacitors after inductor).

NOTE 7 Efficiency calculation equation:  $(V_{OUT} * I_{OUT}) / [(V_{IN\_Bulk} * I_{VIN\_Bulk}) + (V_{IN} * I_{VIN})]$ ; where  $V_{OUT}$ ,  $I_{OUT}$ ,  $V_{IN\_Bulk}$ ,  $I_{VIN\_Bulk}$ ,  $V_{IN}$ ,  $I_{VIN}$  parameters are actual measured values.

NOTE 8 Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature less than or equal to 105 °C). The inductor characteristics noted above applies inductor temperature of 105 °C.

NOTE 9 The output buck regulator switching frequency is set to 750 KHz for SWA/SWB/SWC/SWD. The device under test (DUT) must also comply with all PMIC's electrical characteristics (DC+AC) specifications. The efficiency spec for switching frequency greater or different than 750 KHz for SWA/SWB/SWC/SWD is not specified and it is vendor specific.

NOTE 10 For input supply rail, probing is done at the input high frequency filter cap (0.1  $\mu\text{F}$ ) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.

NOTE 11 Acoustic noise prevention control feature is disabled by setting Table 158, "Register 0x36" [3:1] = '000'.

**3.2.2 VIN\_Bulk = 3.3 V****Table 10 — Efficiency Characteristics; VIN\_Bulk = 3.3V<sup>[1]</sup>**

Switch Node Output	Efficiency (% of Max Itdc Load)						Unit	Notes
	15%	20%	25%	50%	75%	100%		
SWA	≥ 86	≥ 87	≥ 86	≥ 86	≥ 81	≥ 78	%	[2],[3],[4],[5],[6],[7],[8],[9],[10],[11]
SWD	≥ 84	≥ 86	≥ 87	≥ 85	≥ 83	≥ 80	%	
SWB; Vout = 0.5V	≥ 77	≥ 82	≥ 83	≥ 85	≥ 81	≥ 79	%	
SWB; Vout = 0.3V	≥ 67	≥ 70	≥ 72	≥ 79	≥ 76	≥ 72	%	
SWC	≥ 87	≥ 89	≥ 90	≥ 89	≥ 84	≥ 83	%	

NOTE 1 The efficiency numbers assume the inductor specification as noted in Section 7.2.

NOTE 2 The maximum Itdc as specified in Table 4 to Table 7 appropriately.

NOTE 3 When the efficiency of any given output regulator is being measured, all other switching output regulators are disabled.

NOTE 4 No external load on VOUT\_1.8V, VOUT\_1.0V LDO is applied.

NOTE 5 I<sup>2</sup>C/I<sup>3</sup>C Basic bus is pulled High and held static. PWR\_GOOD signal is pulled High and held static.

NOTE 6 The efficiency includes the buck regulator loss, the PCB loss ( $\leq 2.5 \text{ m}\Omega$  from the SWx output pin of the PMIC to VOUTx bulk capacitors after inductor).

NOTE 7 Efficiency calculation equation:  $(V_{OUT} * I_{OUT}) / [(V_{IN\_Bulk} * I_{IN\_Bulk}) + (V_{IN} * I_{IN})]$ ; where  $V_{OUT}$ ,  $I_{OUT}$ ,  $V_{IN\_Bulk}$ ,  $I_{IN\_Bulk}$ ,  $V_{IN}$ ,  $I_{IN}$  parameters are actual measured values.

NOTE 8 Applies at maximum ambient temperature of 65 °C (PMIC Junction temperature less than or equal to 105 °C). The inductor characteristics noted above applies inductor temperature of 105 °C.

NOTE 9 The output buck regulator switching frequency is set to 750 KHz. for SWA/SWB/SWC/SWD. The device under test (DUT) must also comply with all PMIC's electrical characteristics (DC+AC) specifications. The efficiency spec for switching frequency greater or different than 750 KHz for SWA/SWB/SWC/SWD is not specified and it is vendor specific.

NOTE 10 For input supply rail, probing is done at the input high frequency filter cap (0.1  $\mu\text{F}$ ) to PMIC pin. For output rail, probing is done at the output cap location at the inductor load side.

NOTE 11 Acoustic noise prevention control feature is disabled by setting Table 158, "Register 0x36" [3:1] = '000'.

### 3.3 I<sup>2</sup>C or I<sup>3</sup>C Basic DC and AC Electrical Characteristics

**Table 11 — I<sup>2</sup>C, I<sup>3</sup>C Basic and Logic Interface DC Electrical Specification**

Parameter	Symbol	Min	Max	Unit	Notes
Input Low Voltage (PWR_GOOD, SDA, SCL, VR_EN, Unlock, DVFSQ_n, SWB_Disable)	V <sub>IL</sub>	-0.3	0.3	V	
Input High Voltage (SDA, SCL)	V <sub>IH</sub>	0.7	3.6	V	
Input High Voltage (PWR_GOOD, VR_EN, Unlock, DVFSQ_n,)		1.26	3.6	V	
Input High Voltage (SWB_Disable)		1.26	5.5	V	
Output Low Voltage (SDA)	V <sub>OL</sub>	-	0.3	V	
Output Low Voltage (PWR_GOOD, GSI_n)		-	0.3	V	[1]
Output High Voltage (SDA)	V <sub>OH</sub>	0.75	-	V	
Output Low Current (SDA)	I <sub>OL</sub>	3	-	mA	
Output Low Current (PWR_GOOD, GSI_n)		3	-	mA	
Output High Current (SDA)	I <sub>OH</sub>	-	-3	mA	
Rising Output Slew Rate (SDA)	Slew_Rate	0.1	1	V/ns	[2]
Falling Output Slew Rate (SDA)		0.1	3	V/ns	
Input Leakage Current	I <sub>LI</sub>	-	± 5	μA	
Output Leakage Current	I <sub>LO</sub>	-	± 5	μA	

NOTE 1 PWR\_GOOD output is Open Drain output. There is an external pullup resistor to 1.8 V or 3.3 V on the board or other device.

NOTE 2 Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load is shown in Figure 6. Figure 7 shows the timing measurement points. For slew rate measurement, the V<sub>OH</sub> level shown in Figure 7 is a function of R<sub>on</sub> value; V<sub>OH</sub> = {1.0/(R<sub>on</sub> + 50)} \* 50.

**Table 12 — Input Capacitance**

Parameter	Symbol	Min	Max	Unit	Notes
Input Capacitance (PWR_GOOD, SCL, SDA, VR_EN, Unlock, DVFSQ_n, SWB_Disable)	C <sub>IN</sub>	-	5	pF	

**Table 13 — Input Spike Filter**

Parameter	Symbol	Test Condition	Min	Max	Unit	Notes
Pulse width of spikes which must be suppressed by the input filter in I <sup>2</sup> C mode	t <sub>SP</sub>	Single glitch, f < 100 KHz	-	-	ns	
		Single glitch, f > 100 KHz	-	50	ns	[1]

NOTE 1 T<sub>A</sub> = 25 °C; f = 400 KHz. Verified by design and characterization only.

### 3.3 I<sup>2</sup>C or I<sup>3</sup>C Basic DC and AC Electrical Characteristics (cont'd)

**Table 14 — Output Ron**

Parameter	Symbol	Min	Max	Unit	Notes
SDA Output Pullup and Pulldown Driver Impedance	R <sub>ON</sub>	20	100	Ω	[1]
GSI_n, PWR_GOOD Output Pulldown Driver Impedance		20	100	Ω	[2]

NOTE 1 Pulldown Ron = Vout/Iout. Pullup Ron = (VOUT\_1.0V - Vout)/Iout.

NOTE 2 Pulldown Ron = Vout/Iout

**Table 15 — I<sup>2</sup>C and I<sup>3</sup>C Interface AC Characteristics**

Parameter	Symbol	I <sup>2</sup> C Mode - Open Drain		I <sup>3</sup> C Basic Mode Push-Pull[1]		Unit	Notes
		Min	Max	Min	Max		
Clock Frequency	f <sub>SCL</sub>	0.01	1	0.01	12.5	MHz	
Clock High Pulse Width Time	t <sub>High</sub>	260		35		ns	
Clock Low Pulse Width Time	t <sub>Low</sub>	500		35		ns	
Detect Clock Input Low Time	t <sub>TIMEOUT</sub>	10	50	10	50	ms	
Rise Time	t <sub>R</sub>	-	120	-	5	ns	[2],[3]
Fall time	t <sub>F</sub>	-	120	0	5	ns	2,3
Data in Setup Time	t <sub>SU:DAT</sub>	50	-	8	-	ns	2,[4]
Data in Hold Time	t <sub>HD:DI</sub>	0	-	3	-	ns	2,4
Start Condition Setup Time	t <sub>SU:STA</sub>	260	-	12	-	ns	2
Start Condition Hold Time	t <sub>HD:STA</sub>	260	-	30	-	ns	2
Stop Condition Setup Time	t <sub>SU:STO</sub>	260	-	12	-	ns	2
Time between Stop Condition and next Start Condition	t <sub>BUF</sub>	500	-	500	-	ns	2,[5]
SDA Data Out Hold Time	t <sub>HD:DAT</sub>	0.5	350	N/A	N/A	ns	[6]
SCL Falling Clock In to Valid SDA Data Out Time	t <sub>DOUT</sub>	N/A	N/A	0.5	12	ns	[7],[8]
SCL Rising Clock In to Target SDA Output Off	t <sub>DOFFT</sub>	N/A	N/A	0.5	12	ns	8,[9]
SCL Rising Clock In to Controller SDA Output Off	t <sub>DOFFC</sub>	N/A	N/A	0.5	30	ns	8,[10]
SCL Rising Clock In to Controller Driving Data Signal Low	t <sub>CL_r_DAT_f</sub>	N/A	N/A	40	-	ns	[11]
Bus Available Time (no edges seen on SCL and SDA)	t <sub>AVAIL</sub>	N/A	N/A	1	-	μs	
Time to issue IBI after an event is detected when Bus is available	t <sub>IBI_ISSUE</sub>	N/A	N/A	-	15	μs	

**Table 15 — I<sup>2</sup>C and I3C Interface AC Characteristics (cont'd)**

Parameter	Symbol	I <sup>2</sup> C Mode - Open Drain		I3C Basic Mode Push-Pull <sup>[1]</sup>		Unit	Notes
		Min	Max	Min	Max		
Time from Clear Register Status to any I3C operation with Start condition to avoid false IBI generation; PEC disabled	$t_{CLR\_I3C\_CMD\_Delay}$	N/A	N/A	4	-	μs	
Time from Clear Register Status to any I3C operation with Start condition to avoid false IBI generation; PEC enabled		N/A	N/A	15	-	μs	
DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay	$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	3	-	3	-	μs	[12],[13], [14]
Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode	$t_{WR\_RD\_DELAY\_PEC\_EN}$	N/A	N/A	8	-	μs	[15],[16], [17]
SETHID CCC or SETAASA CCC followed by any other CCC or Read/Write Command Delay	$t_{I2C\_CCC\_Update\_Delay}$	2.5	-	N/A	N/A	μs	
RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command Delay	$t_{I3C\_CCC\_Update\_Delay}$	-	-	2.5	-	μs	
Any CCC followed by RSTDAA CCC Delay	$t_{CCC\_Delay}$	N/A	N/A	2.5	-	μs	

NOTE 1 I3C Basic mode with Open Drain operation follows timing values as shown in I<sup>2</sup>C Mode - Open Drain column.

NOTE 2 See Figure 3 for PMIC's input timing definition.

NOTE 3 See Figure 8 for voltage threshold definition for rise and fall times.

NOTE 4 The input setup time is referenced from SDA VIL or VIH threshold as shown in Figure 3 to SCL VIH threshold as shown in Figure 3. The input hold time is referenced from SCL VIL threshold as shown in Figure 3 to SDA VIL or VIH threshold as shown in Figure 3.

NOTE 5 If PEC is enabled,  $t_{WR\_RD\_DELAY\_PEC\_EN}$  timing parameter applies.

NOTE 6 The PMIC device guarantees  $t_{HD:DAT}$  value in I<sup>2</sup>C mode of operation. See Figure 5 for PMIC's output timing definitions as well as SCL clock input threshold level and SDA data output threshold levels.

NOTE 7 The PMIC device must be configured in I3C Basic mode to guarantee  $t_{DOUT}$  value. See Figure 4 for PMIC's output timing definition as well as SCL clock input threshold level and SDA data output threshold levels.

NOTE 8 This timing parameter is guaranteed into output timing reference load as shown in Figure 6.

NOTE 9 The PMIC device must be configured in I3C Basic mode to guarantee  $t_{DOFFT}$  value. See Figure 32.

NOTE 10 The PMIC device must be configured in I3C Basic mode to guarantee  $t_{DOFFC}$  value. See Figure 33.

NOTE 11 See Figure 34.

NOTE 12 From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.

NOTE 13 The PMIC sends NACK if Host does not satisfy  $t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$  timing parameter.

NOTE 14 This timing parameter restriction is only applicable when PEC function is disabled in PMIC. If PEC is enabled, this timing parameter does not apply.

NOTE 15 From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.

NOTE 16 This timing parameter restriction is only applicable when PEC function is enabled in PMIC. If PEC is disabled, this timing parameter does not apply.

NOTE 17 The PMIC sends NACK if Host does not satisfy  $t_{WR\_RD\_DELAY\_PEC\_EN}$  timing parameter.

### 3.3 I<sup>2</sup>C or I<sup>3</sup>C Basic DC and AC Electrical Characteristics (cont'd)

The PMIC follows the I<sup>2</sup>C bus and I<sup>3</sup>C Basic bus input timing requirements as shown in Figure 3 and Table 15 and output timing requirement as shown in Figure 4.

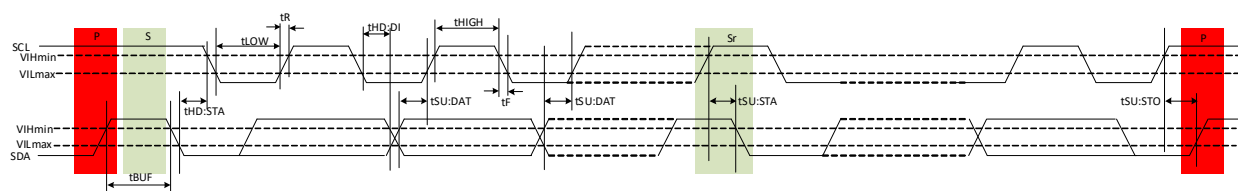


Figure 3 — I<sup>2</sup>C or I<sup>3</sup>C Basic Bus AC Input Timing Parameter Definition

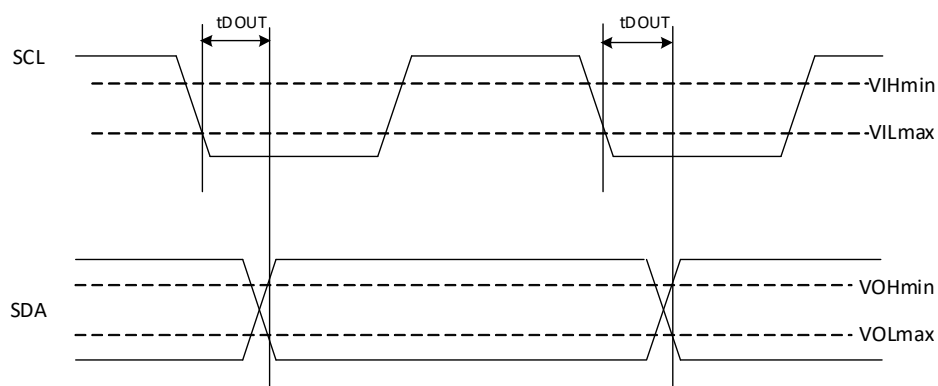


Figure 4 — I<sup>3</sup>C Basic Bus AC Output Timing Parameter Definition

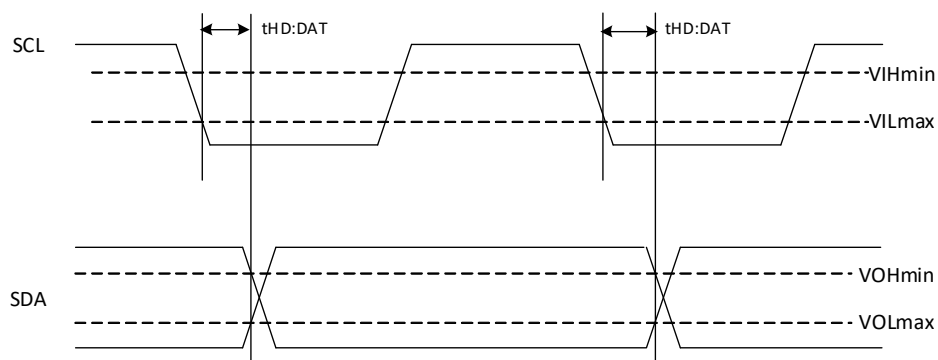


Figure 5 — I<sup>2</sup>C Bus AC Output Timing Parameter Definition



### 3.3 I<sup>2</sup>C or I<sup>3</sup>C Basic DC and AC Electrical Characteristics (cont'd)

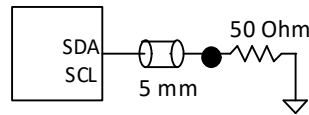


Figure 6 — Output Slew Rate and Output Timing Reference Load

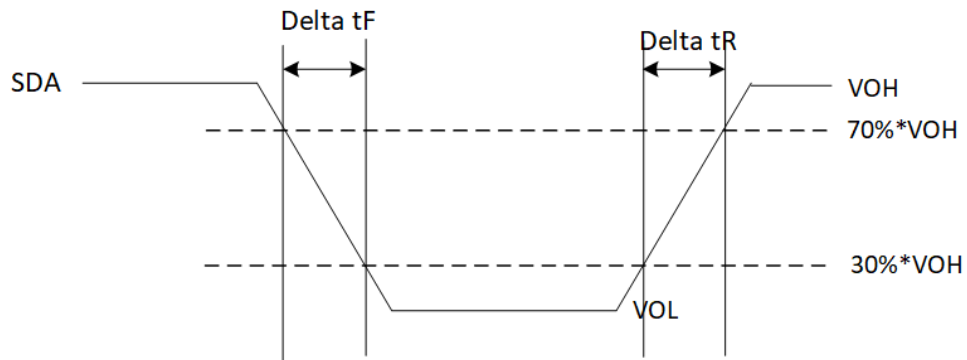


Figure 7 — Output Slew Rate Measurement Points

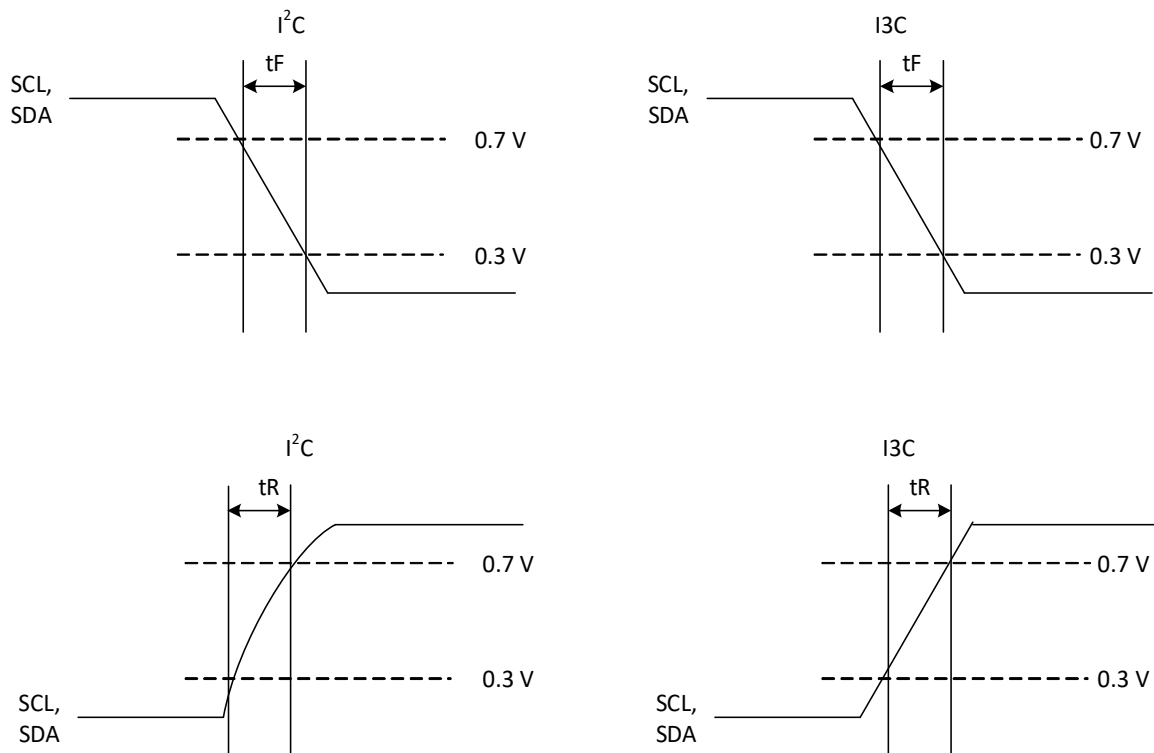


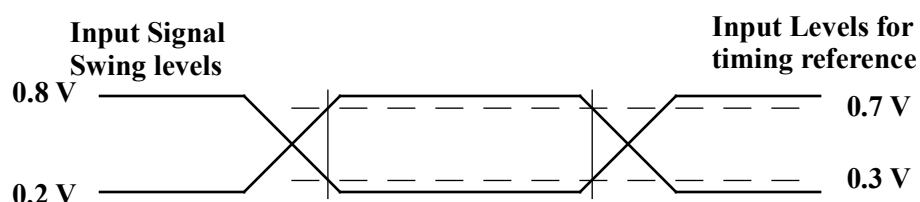
Figure 8 — Input Rise and Fall Timing Parameter Definition

### 3.4 Measurement Condition

**Table 16 — AC Measurement Conditions [1]**

Symbol	Parameter	Min	Max	Units
C <sub>L</sub>	Load capacitance		40	pF
	Input rise and Fall times - Open Drain	-	120	ns
	Input rise and fall times - Push Pull	-	5	ns
	Input signal swing levels	0.2 to 0.8		V
	Input levels for timing reference	0.3 to 0.7		V

NOTE 1 These AC measurement conditions (Table 16 and Figure 9) are for lab test purposes only.



**Figure 9 — AC Measurement Waveform**

### 3.5 PMIC AC Timing Parameters

**Table 17 — PMIC Timing Parameters**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Supply to GSI_n assertion	tInput_PWR_GOOD_GSI_Assertion	-	-	10	μs	
Input supply over voltage condition to GSI_n assertion	tInput_OV_GSI_Assertion	-	-	10	μs	
Input over voltage condition to automatic PMIC VR Disable	tInput_OV_VR_Disable	-	-	20	μs	
Output Voltage Tolerance to GSI_n assertion	tOutput_PWR_GOOD_GSI_Assertion	-	-	10	μs	
Output over voltage condition to automatic PMIC VR Disable	tOutput_OV_VR_Disable	-	-	20	μs	
Output under voltage lockout condition to automatic PMIC VR Disable	tOutput_UV_VR_Disable	-	-	20	μs	
Output current limiter warning to GSI_n assertion	tOutput_Current_Limiter	-	-	10	μs	

**Table 17 — PMIC Timing Parameters (cont'd)**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
High temperature warning to GSI_n assertion	tHigh_Temp_Warning	-	-	10	μs	
Critical Temperature condition to automatic PMIC shut down	tShut_Down_Temp	-	-	10	μs	
VIN_Bulk input supply stable to VR Enable Command	tVIN_Bulk_to_VR_Enable	6.5	-	-	ms	
VIN_Bulk input supply stable to VOUT_1.8V output stable	t1.8V_Ready	-	-	2.5	ms	
VOUT_1.8V output supply stable to VOUT_1.0V output stable	t1.0V_Ready	-	-	1.0	ms	[1]
VOUT_1.8V output supply to PMIC Management Ready	tManagement_Ready	-	-	3	ms	
VR Enable Command to PMIC output regulator ready	tPMIC_PWR_Good_Out	Figure 15			ms	
VR Disable Command to PMIC Output Regulators Off	tPMIC_Output_Off	Figure 21			ms	
PWR_GOOD, Unlock Input Low Pulse Width	tPWR_GOOD_Low_Pulse_Width	2	-	-	μs	
Minimum DVFSQ_n Input High or Input Low Pulse Width	tHigh_Pulse:DVFSQ_n tLow_Pulse:DVFSQ_n	5	-	-	μs	[2],[3]
PWR_GOOD, Unlock, DVFSQ_n, Input Low Pulse Width Input Filter	tPWR_GOOD_Low_Pulse_Width_Filter	-	-	0.35	μs	
VR_EN Input High Pulse Width	tVR_EN_High_Pulse_Width	2			μs	
VR_EN Input High Pulse Width Input Filter	tVR_EN_High_Pulse_Width_Filter	-	-	0.35	μs	
Output Voltage Adjustment in Programmable Mode	$\Delta v/\Delta t$	-	1	-	mV/μs	[4]
PMIC Delay from DVFSQ_n input signal reaching High threshold until SWB output voltage begins to slew high	tDelay_DVFSQ_HI_VSLEW	-	-	5	μs	[5]
PMIC Delay from DVFSQ_n input signal reaching Low threshold until SWB output voltage begins to slew low	tDelay_DVFSQ_LO_VSLEW	-	-	5	μs	[5]
SWB output voltage slew rate upon entry and exit from DVFSQ state	DVFSQ_VOLTAGE_SLEW_RATE	-10		+10	mV/μs	[5],[6],[7],[8]
SWB_Disable setup time prior to VR_EN Pin Assertion to High	tSU:SWB_Disable_VR_EN	10	-	-	μs	
SWB_Disable hold time after VR_EN Pin Assertion to High	tHD:SWB_Disable_VR_EN	10	-	-	μs	
Unlock setup time prior to VR_EN assertion or I2C/I3C Bus command	tSU:Unlock	10	-	-	μs	

**Table 17 — PMIC Timing Parameters (cont'd)**

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unlock hold time after VR_EN assertion or I2C/I3C Bus command	tHD:Unlock	10	-	-	μs	
Minimum Unlock InputHigh or Input Low time pulse width	tHigh_Pulse:Unlock tLow_Pulse:Unlcok	20			μs	[9]

NOTE 1 This time is added to  $t_{1.8V\_Ready}$  parameter to get total time from VIN\_Bulk input supply.

NOTE 2 The controller is not permitted to change the status of the DVFSQ\_n input signal while the SWB output voltage is slewing. The controller must assert the DVFSQ\_n input signal longer than the sum of PMIC slew delay and the SWB output voltage transition time which is defined by the equation:  $t_{Signal\_to\_slew\_delay} + \{SWB\_Voltage\_Setting - SWB\_DVFSQ\_Voltage\_Setting\} / 0.9 * SWB\_DVFSQ\_Voltage\_Slew\_Rate$

NOTE 3 See [Figure 10](#)

NOTE 4 See footnote 4 for registers [Table 137, "Register 0x21," \[7:1\]](#), [Table 139, "Register 0x23," \[7:1\]](#), [Table 141, "Register 0x25," \[7:1\]](#), and [Table 143, "Register 0x27," \[7:1\]](#). The accuracy is  $\pm 10\%$ .

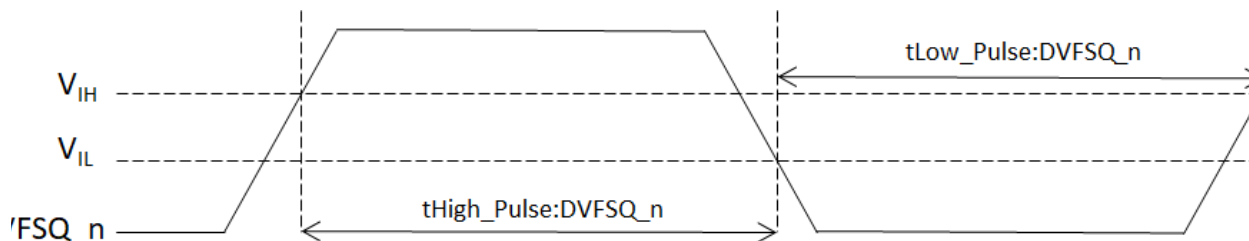
NOTE 5 See [Figure 11](#)

NOTE 6 Typical value as configured in [Table 150, "Register 0x2E" \[7:6\]](#).

NOTE 7 The SWB DVFSQ slew rate is measured from 20% to 80% of the output voltage swing as shown in [Figure 11](#).

NOTE 8 During SWB output voltage transitions, once the output voltage crosses the programmed value, the output voltage must reside within the SWB output voltage tolerance limits.

NOTE 9 See [Figure 12](#)



**Figure 10 — DVFSQ\_n Pin Minimum High and Low Pulse Width**

### 3.5 PMIC AC Timing Parameters (cont'd)

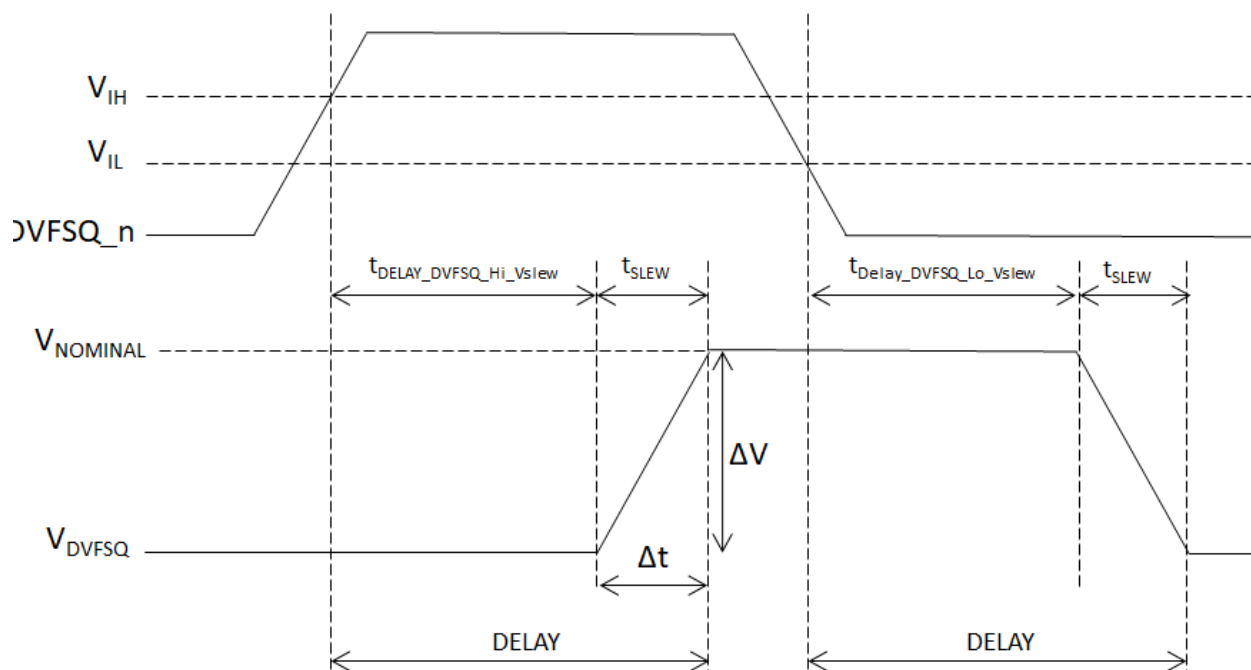


Figure 11 — Delay from DVFSQ\_n Pin to SWB Output Regulator Begins to Slew

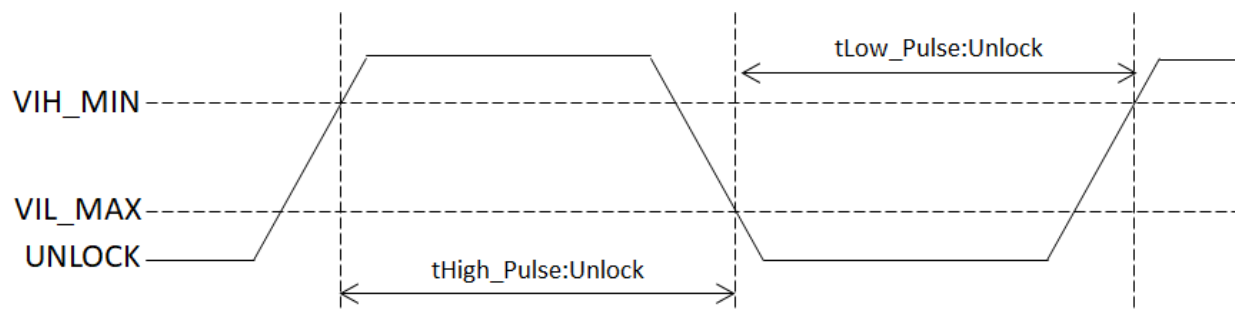


Figure 12 — Unlock Pin Minimum High and Low Pulse Width

### 3.6 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 18, “Absolute Maximum Rating” and Table 19, “ESD Requirement”, and Table 20, “EOS Requirement” may cause permanent damage to the device. Functional operation of PMIC5200 at absolute maximum ratings is not implied. Exposure to absolute maximum rating condition for extended periods may affect long term reliability.

**Table 18 — Absolute Maximum Rating**

Pin	Maximum Rating		Unit
	DC	AC	
VIN_BULK, VIN, SWB_Disable	-0.3 to 6	TBD (Duration $\leq$ 25 ns)	V
VOUT_1.8V, VOUT_1.0V	-0.3 to 2.2	-	V
SWA, SWD, SWB, SWC	-0.3 to 6	-3 to 9 (Duration < 25 ns)	V
BOOT_SWA, BOOT_SWD, BOOT_SWB, BOOT_SWC (to GND)	-0.3 to 12	-0.3 to 15 (Duration < 25 ns)	V
BOOT_SWA, BOOT_SWD, BOOT_SWB, BOOT_SWC (to SWx)	-0.3 to 6	TBD	V
SWA_FB, SWD_FB, SWB_FB, SWC_FB (to AGND)	-0.3 to 2.2	-	V
PWR_GOOD, GSI_n, VR_EN, Unlock, DVFSQ_n	-0.3 to 5.0	-	V
SCL, SDA; I <sup>2</sup> C Mode only	-0.3 to 5.0		
SCL, SDA; I <sup>3</sup> C Mode only	-0.3 to 2.1		
PID	-0.3 to 2.2	TBD	V
AGND, PGND	-0.3 to 0.3	-	V

### 3.7 ESD Requirements

**Table 19 — ESD Requirement**

Test Model	Pin	Maximum Rating	Unit
HBM	All	$\pm 2000$	V
CDM	All	$\pm 500$	V

**Table 20 — EOS Requirement**

Pin	Maximum Rating	Unit	Notes
VIN_BULK	10	V	[1],[2],[3],[4]

NOTE 1 The test is performed on PMIC5200 without any input capacitor on VIN\_BULK

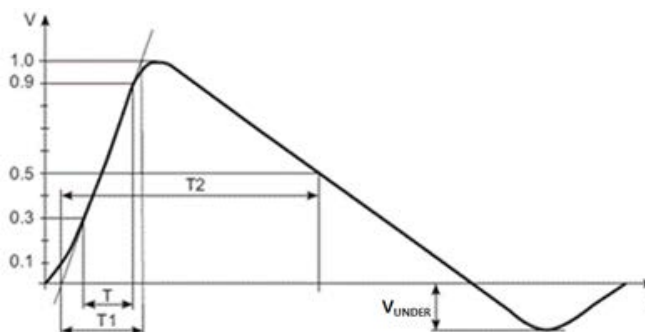
NOTE 2 The input source needs to follow the waveform and condition as shown in [Figure 13](#) and [Table 21](#).

NOTE 3 Probing is performed at the VIN\_BULK pin of PMIC.

NOTE 4 Applies to VIN\_Bulk and VIN pin.

**Table 21 — Input Source Condition**

Item	Value	Notes
T (rise from 30% to 90% of peak)	$0.72 \mu\text{s} (+30\%)$	
T1 (rise time)	$1.2 \mu\text{s} (+30\%)$	$T1 = 1.67 \cdot T$
T2 (duration time to half value)	$50 \mu\text{s} (+20\%)$	
Output Impedance	$2 \Omega$	
V <sub>UNDERSHOOT</sub> Voltage	30% Max	



**Figure 13 — Impulse Waveform for EOS Test (IEC 61000-4-5)**

### 3.8 Thermal Characteristics

**Table 22 — Thermal Characteristics**

Parameter	Symbol	Maximum Rating	Unit	Notes
Thermal resistance junction to case	$\Theta_{JC}$	TBD	$^{\circ}\text{C}/\text{W}$	[1],[2],[3]
Junction operating temperature	$T_J$	-10 to 125	$^{\circ}\text{C}$	
Case operating temperature	$T_C$	-10 to TBD	$^{\circ}\text{C}$	3
Storage temperature	$T_{STG3}$	-55 to 150	$^{\circ}\text{C}$	3
Lead temperature (soldering, 10s)	$T_{LEAD}$	260	$^{\circ}\text{C}$	3

NOTE 1 The maximum power dissipation is  $P_{D(MAX)} = (T_{JMAX} - T_C) / \Theta_{JC}$ . Exceeding the maximum allowable power dissipation results in excessive die temperature and the device will enter thermal shutdown.

NOTE 2 This thermal rating was calculated on JEDEC 51 standard 4 layer board with dimensions 3" x 4.5" in still air conditions. Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude and other unlisted variables.

NOTE 3 This specification is compliant with JESD402-1 Temperature Grade and Measurement Specification for Components and Modules, operating temperature range MT, storage temperature range  $T_{STG3}$ . See JESD402-1 for details, including measurement point.



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## 4 Functional Operation

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### 4.1 PMIC Input Voltage Supply and Ramp Condition

The PMIC5200 has one input supply from the platform: VIN\_Bulk.

The VIN\_Bulk supply is used by the PMIC for all four switch (SWA, SWB, SWC, SWD) output regulators and two LDO outputs (VOUT\_1.8V and VOUT\_1.0V) regulators. Note that the VOUT\_1.8V LDO output is separate and independent from SWC output, which is for the DRAM VPP rail. The VOUT\_1.0V LDO output is separate and independent from SWA or SWB.

At first power on, the VIN\_Bulk input supply shall reach a minimum threshold voltage of 3.0V before it can be detected as a valid input supply to the PMIC.

Once the VIN\_Bulk supply is valid and stable (i.e., above 3.0 V), the PMIC shall assert PWR\_GOOD output low, drive VOUT\_1.8V and VOUT\_1.0V supply within  $t_{1.8V\_Ready}$  and  $t_{1.0V\_Ready}$  time respectively. The PMIC drives PWR\_GOOD output signal low only when VIN\_Bulk input supply reaches minimum of 3.0V. The PWR\_GOOD output is pulled up to either 1.8 V or 3.3 V on the platform or on the host controller.

The PWR\_GOOD pullup voltage (either 1.8 V or 3.3 V) can be available before or after VIN\_Bulk is valid and stable. If PWR\_GOOD pullup voltage is available before VIN\_Bulk is applied, the PWR\_GOOD signal is High and remains High with no leakage path or damage to the PMIC. When VIN\_Bulk is applied to the PMIC, the PMIC asserts PWR\_GOOD output low. The platform should pay attention to timing relationship between PWR\_GOOD pullup voltage and VIN\_Bulk ramp to prevent undesired glitches on PWR\_GOOD signal.

The PMIC shall enable I<sup>2</sup>C/I<sup>3</sup>C bus interface function within tManagement\_Ready. The host shall not attempt to access the PMIC's memory registers until tManagement\_Ready timing requirement is satisfied.

### 4.2 Power Up Initialization Sequence

During power on, the host shall:

1. Ramp up VIN\_Bulk supply.
2. Hold VIN\_Bulk supply stable for a minimum of tVIN\_Bulk\_to\_VR\_Enable time.
3. Hold VR\_EN pin to static low or high. There is no timing relationship required on VR\_EN pin with respect to VIN\_Bulk input supply ramp up as long as VR\_EN pin is held to static level to either low or high.
4. During VIN\_Bulk ramp, if VR\_EN signal is held low, it can transition to high only once for normal operation. Once high, it shall remain high. The VR\_EN signal is not allowed to transition to low during VIN\_Bulk ramp up. An exception is allowed when the platform suffers unexpected power loss during VIN\_Bulk ramp. For this exception case, the PMIC shall guarantee normal operation at subsequent successful power up ramp. There is no limit how many times this exceptional condition can occur at the platform level and hence PMIC shall be responsible to guarantee normal operation at subsequent successful power up ramp.
5. If VR\_EN pin is held High during VIN\_Bulk ramp up or transitions to High during VIN\_Bulk ramp up, the PMIC turns on its output rails.
6. If VR\_EN pin is held Low during VIN\_Bulk Ramp, assert VR\_EN signal High to turn on PMIC output rails. Alternatively, host can issue VR Enable command by setting register [Table 154, Register 0x32 \[7\] = '1'](#) via I<sup>2</sup>C/I<sup>3</sup>C Basic bus or via DEVCTRL CCC to turn on PMIC output rails.

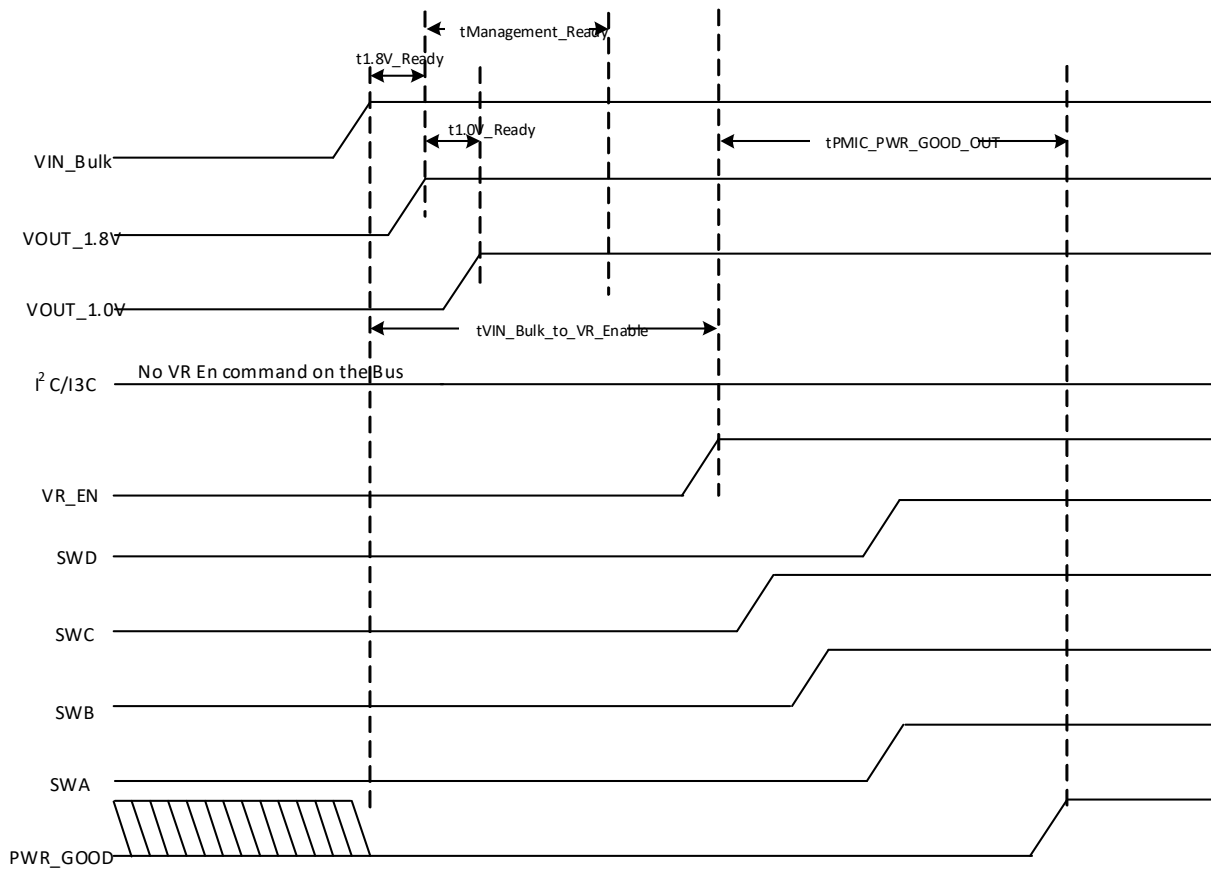
#### 4.2.1 Power Up Sequence

Figure 14 to Figure 17 show examples of PMIC power up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB, SWC, SWD) is for example purpose only. The specific ramp up sequence is configurable through power on sequence configuration registers.

After VR Enable command is registered on the I<sup>2</sup>C or I<sup>3</sup>C Basic bus or VR\_EN pin is registered high, the PMIC shall complete the following steps within tPMIC\_PWR\_GOOD\_OUT:

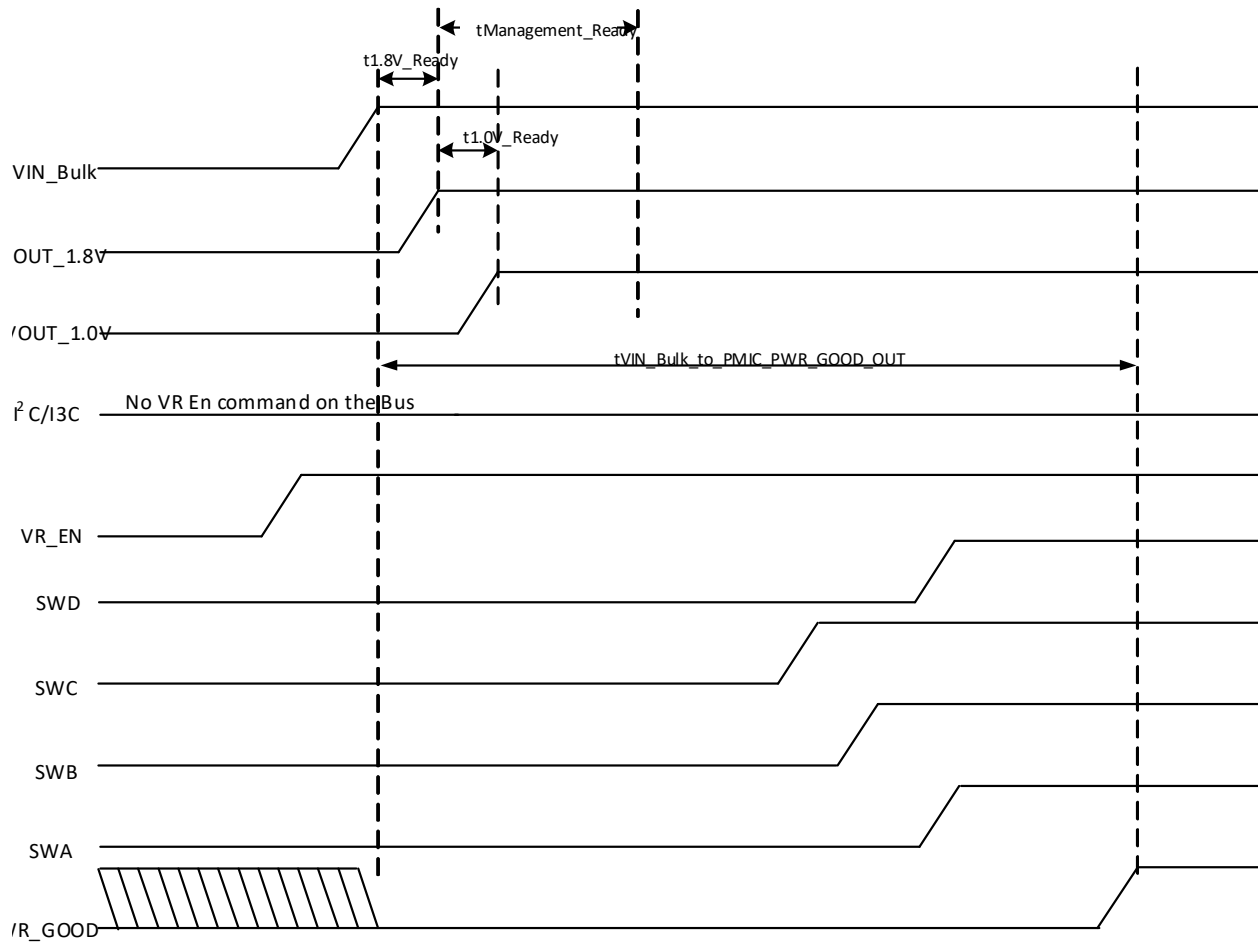
1. Check VIN\_Bulk Power Good status is valid.
2. Power up itself - PMIC executes Power On Sequence Config 0 (Table 182, Register 0x40) to Power On Sequence Config 3 (Table 185, Register 0x43) registers and configures PMIC internal registers as programmed in PMIC5200 vendor memory space registers.
3. Power up all enabled output switch regulators and ready for normal operation
4. Update status registers Table 112, Register 0x08 [5:2] and floats PWR\_GOOD signal within maximum of tPMIC\_PWR\_GOOD\_OUT time.

If PMIC PWR\_GOOD signal is not floated within tPMIC\_PWR\_GOOD\_OUT time, the host can access the PMIC status registers for detailed information after tPMIC\_PWR\_GOOD\_OUT time. The PMIC may NACK for any host request on I<sup>2</sup>C or I<sup>3</sup>C Basic bus after VR Enable command (either with VR\_EN pin high or on I<sup>2</sup>C/I<sup>3</sup>C Basic Bus) until tPMIC\_PWR\_GOOD\_OUT time expires.



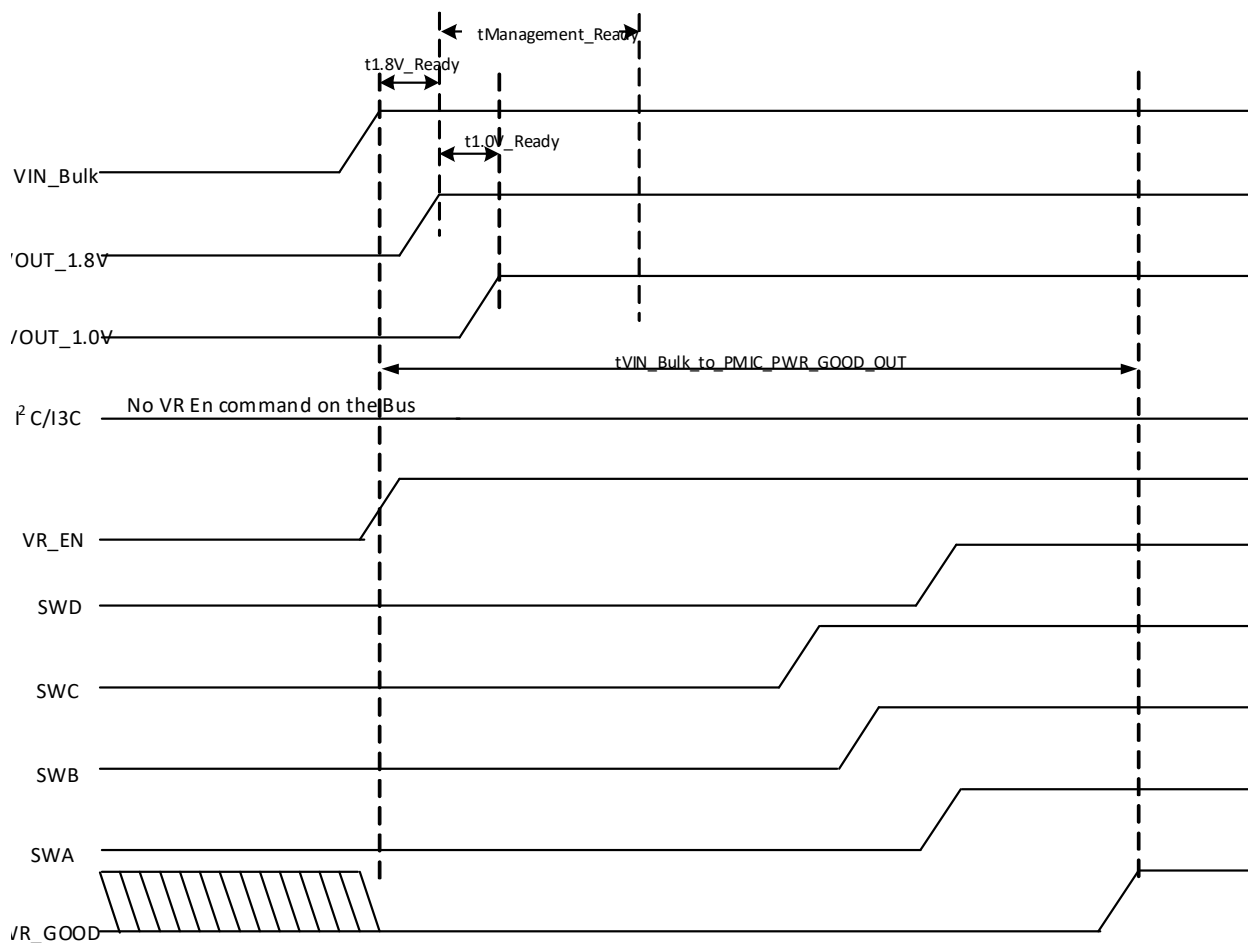
**Figure 14 — Power Up Sequence; VR\_EN Pin High after VIN\_Bulk Ramp; No Bus Command**

#### 4.2.1 Power Up Sequence (cont'd)



**Figure 15 — Power Up Sequence; VR\_EN Pin High before VIN\_Bulk Ramp; No Bus Command**

#### 4.2.1 Power Up Sequence (cont'd)



**Figure 16 — Power Up Sequence; VR\_EN Pin High during VIN\_Bulk Ramp; No Bus Command**

#### 4.2.1 Power Up Sequence (cont'd)

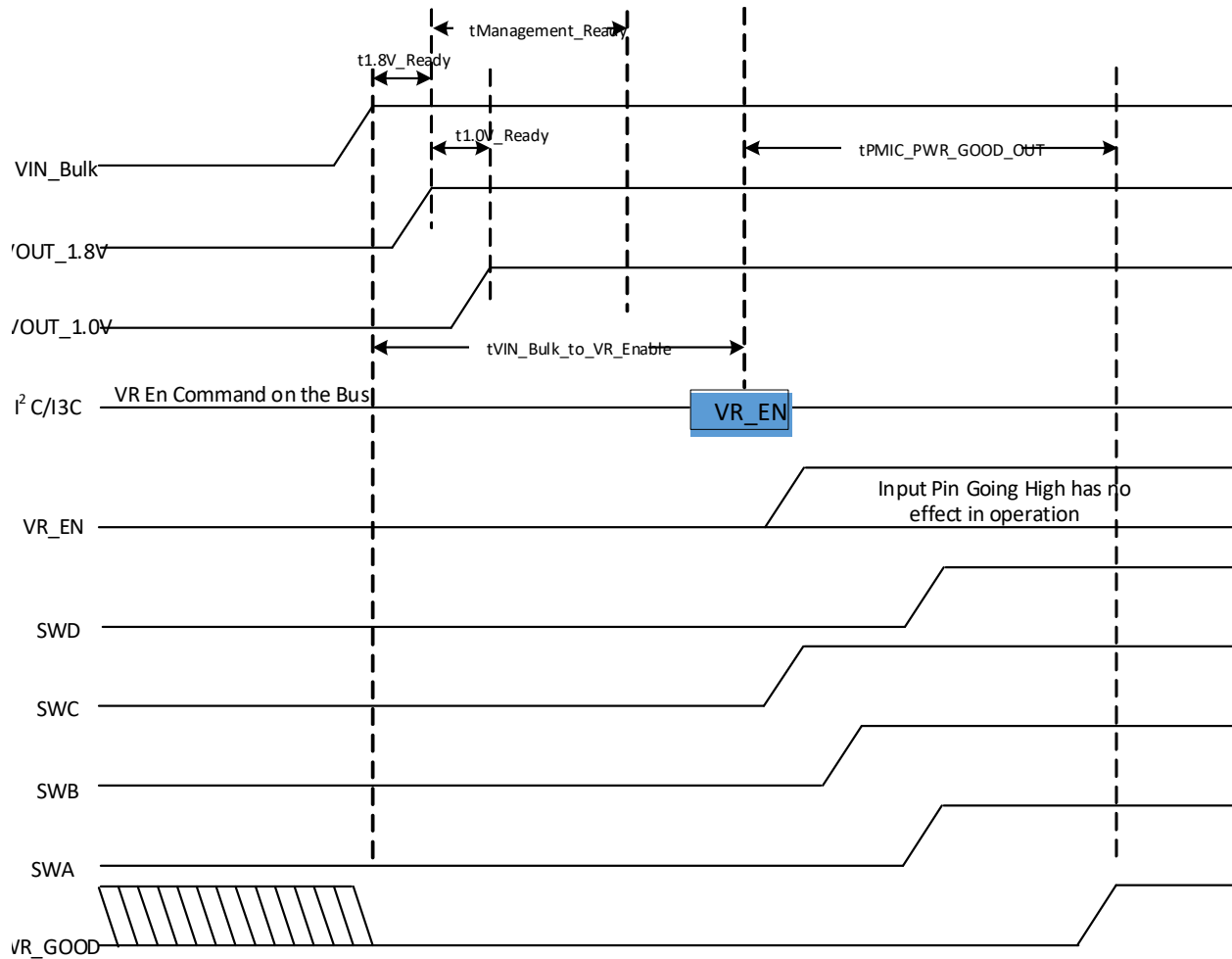


Figure 17 — PMIC Power Up Sequence; with Bus Command

## 4.2.1 Power Up Sequence (cont'd)

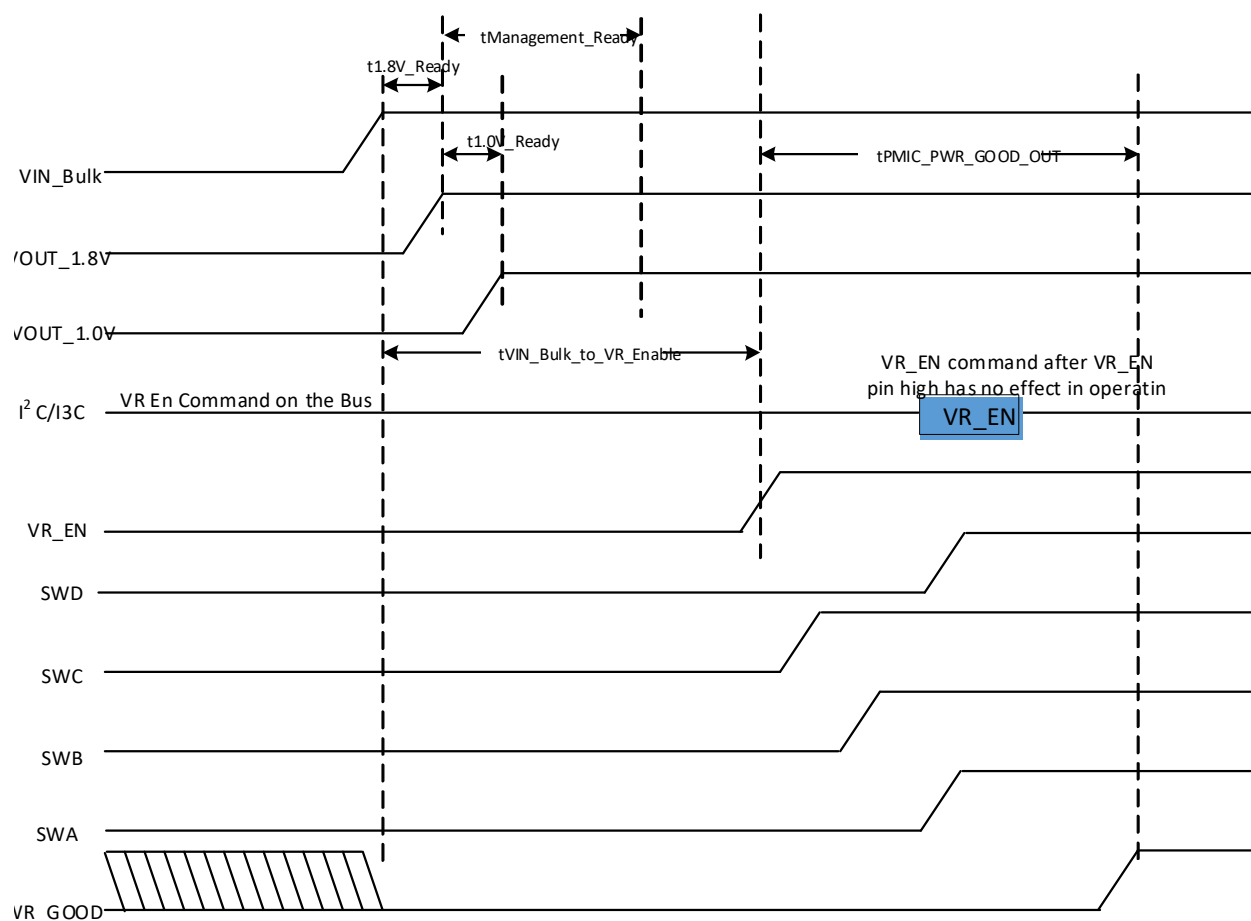


Figure 18 — PMIC Power Up Sequence; with VR\_EN Pin followed by Bus Command

## 4.3 PMIC Output Rail Turn On Timing

Figure 19 shows the timing relationship once the PMIC receives VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus) and when it floats PWR\_GOOD output signal; timing parameter  $t_{PMIC\_PWR\_GOOD\_OUT}$  applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence configuration registers that are executed plus additional 5 ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config3 registers. Note that if more than one regulator are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 19 uses three power on sequence config0 to config3 registers and only one buck regulator is enabled in each power on sequence config 0 to config 3 registers.

### 4.3 PMIC Output Rail Turn On Timing (cont'd)

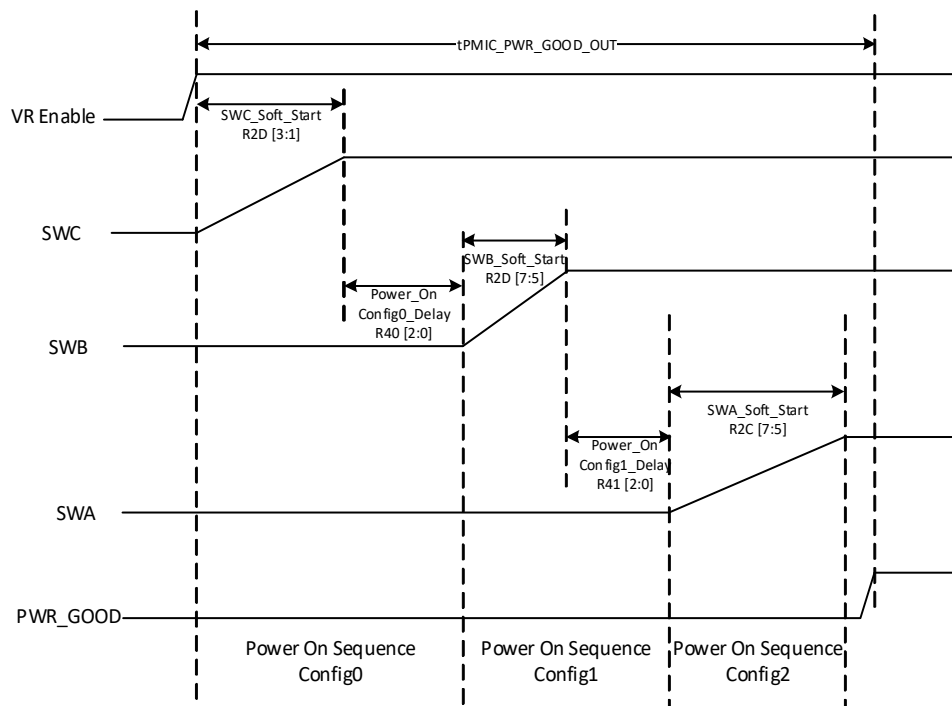


Figure 19 — PMIC Power On Timing

### 4.4 Auto Power On

The PMIC offers auto power on feature by setting [Table 206, Register 0x5F \[6\] = '1'](#). When this feature is enabled, the PMIC automatically executes the VR Enable command (i.e., [Table 154, Register 0x32 \[7\] = '1'](#)) after VIN\_Bulk input supply reach at stable valid level. The PMIC executes power on sequence configuration registers ([Table 182, Register 0x40](#) to [Table 185, Register 0x43](#)) and floats PWR\_GOOD signal.

When the [Table 206, Register 0x5F \[6\] = '1'](#) is burned in the PMIC5200 vendor region, the PMIC requires valid stable VIN\_Bulk input supply. However, first time when this register is burned, the PMIC does not execute the VR Enable command (i.e., [Table 154, Register 0x32 \[7\] = '1'](#)) even though valid VIN\_Bulk input supply is present. The PMIC requires complete power cycle in order to take the effect of burning the [Table 206, Register 0x5F \[6\] = '1'](#).

### 4.5 Secure Mode and Programmable Mode of Operation

Prior to issuing VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus), the host must configure the register [Table 151, Register 0x2F \[2\]](#) appropriately as desired. The PMIC offers two modes of operation after VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus) is registered.

## 4.5 Secure Mode and Programmable Mode of Operation (cont'd)

1. Programmable Mode - In this mode, independent of when host issues VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus), the PMIC allows modification to any register in the host region as desired by the host and PMIC responds appropriately.
2. Secure Mode - In this mode, after host issues VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus), the PMIC does not allow modification to registers [Table 125, Register 0x15](#) to [Table 151, Register 0x2F](#), [Table 154, Register 0x32](#) [7,5:0] in the host region as well as [Table 182, Register 0x40](#) to Register 0x6F in the CAMM2 vendor region. These registers are write-protected and marked with RED color cells in “Register” column in [Table 107, Host Region - Register Map](#) and in [Table 181, CAMM2 Vendor Region - Register Map](#). The PMIC simply ignores the host request. Throughout this entire specification, when it refers to PMIC allowing access to the registers, it refers to write operation to the registers that are not write protected in secure mode or programmable mode. There is no restriction for the read operation in secure mode or programmable mode. The host must power cycle the PMIC to make any modification. The PMIC power cycle is defined as complete removal of VIN\_Bulk input supply to the PMIC and this definition is applied to the entire specification. The PMIC does allow modification to any other remaining registers that are not marked in RED color cells in “Register” column in [Table 107, Host Region - Register Map](#) with I<sup>2</sup>C or I<sup>3</sup>C Basic bus. The Secure Mode is only applicable once VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus) is registered. This is important because by default [Table 151, Register 0x2F](#) [2] = ‘0’ when PMIC is first powered up. Prior to VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus), PMIC allows modification to any registers in the host region.

Note that there is one exception in Secure mode of operation. The exception is for register [Table 154, Register 0x32](#) [7]. This register can get updated with VR\_EN pin assertion/de-assertion or PWR\_GOOD signal input assertion to low or when PMIC internally generates its own VR Disable command due to some fault condition. This register cannot be updated with I<sup>2</sup>C or I<sup>3</sup>C Basic bus command or with DEVCTRL CCC command.

## 4.6 Power Down Output Regulators

Regardless of how PMIC's output regulators are turned on (w/ VR\_EN pin or w/ VR Enable command on I<sup>2</sup>C/I<sup>3</sup>C Basic bus), the PMIC's output regulators are powered down as described below depending on PMIC's mode of operation.

### 4.6.1 Normal Power Down Sequence

Under normal operating conditions with valid VIN\_Bulk input supply, to disable the PMIC output regulators, the PMIC allows following three methods for normal power down sequence.

- VR\_EN pin de-assertion from High to Low
- VR Disable command on I<sup>2</sup>C or I<sup>3</sup>C bus (if PMIC registers are not in secure mode)
- PWR\_GOOD input from High to Low (if PWR\_GOOD pin is configured as IO)

All three methods triggers the PMIC to generate internal VR Disable command and the PMIC executes the normal power down sequence as programmed in Power Off Sequence Config0 to Power Off Sequence Config3 registers ([Table 200, Register 0x58](#) [7:0] to [Table 203, Register 0x5B](#) [7:3]) in DIMM vendor region MTP memory.



#### 4.6.1 Normal Power Down Sequence (cont'd)

The PMIC requires valid VIN\_Bulk input supply (i.e., minimum of 3.0 V) to execute normal power down sequence. In a platform where VIN\_Bulk input supply ramp down rate is very slow (starting from VIN\_Bulk nominal condition of 5 V until it ramps down to 3.0 V), the PMIC may be able to execute normal power down sequence before VIN\_Bulk input supply is completely removed depending on the ramp down rate and programmed soft stop time and delay time in Power Off Sequence Config registers. If the VIN\_Bulk ramp down is very fast (e.g., instantaneous with 0 ns), the PMIC cannot execute normal power down sequence to turn off all buck regulators.

Figure 20 shows one example of normal power down sequence where PMIC regulators are turned off by de-asserting VR\_EN pin from high to low. The PMIC executes Power Off Sequence Config0 to Power Off Sequence Config3 registers (Table 200, Register 0x58 to Table 203, Register 0x5B). The example shows the power down sequence spread out over all four Power Off Sequence Config (0 to 3) registers where only one buck regulator is turned off in each Power Off Sequence Config register. The sequence shows the order where SWA is turned off first followed by delay, then SWB is turned off followed by delay, then SWC is turned off followed by delay, and at last SWD is turned off. Each buck regulator follows its own timing for soft stop time as configured.

The PMIC allows any combination where all four buck regulators can be turned off only in first Power Off Sequence Config0 registers or one or more buck regulators are turned off in any given Power Off Sequence Config registers. The PMIC also allows where no buck regulator is turned off in any Power Off Sequence Config to insert additional delay between Power Off Sequence Config registers.

See additional details about PMIC register status, PWR\_GOOD signal as noted in Section 4.6.2 to Section 4.6.5 depending on how PMIC is configured to operate in normal mode.

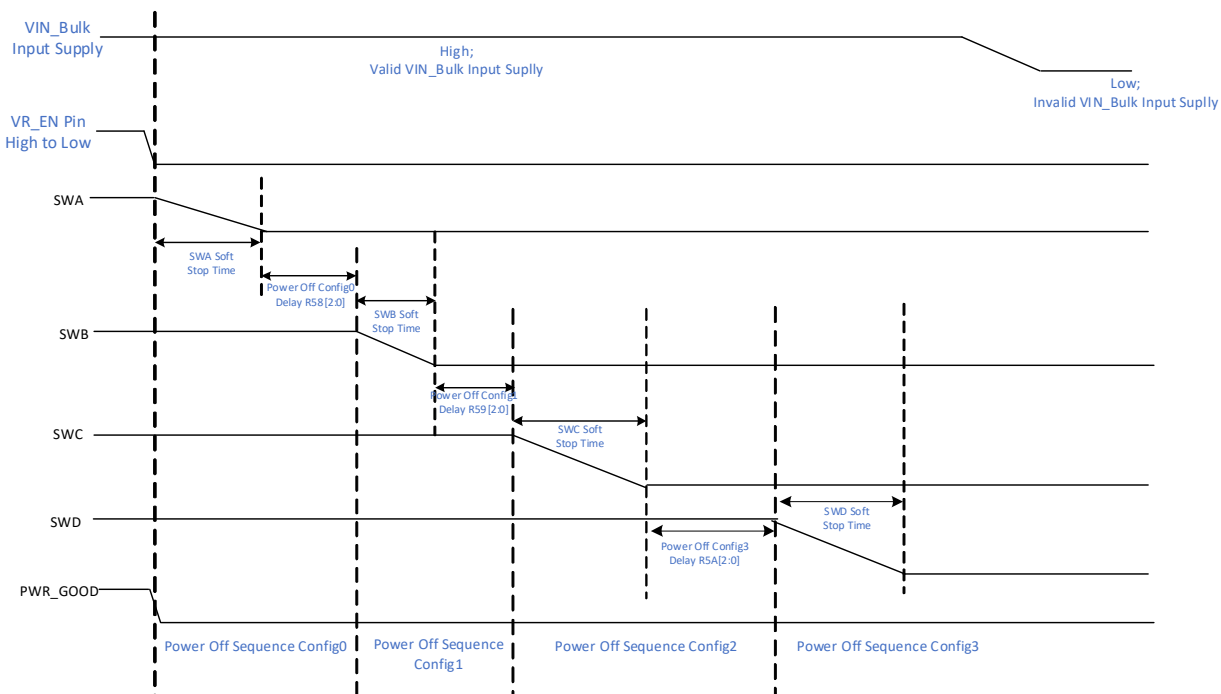


Figure 20 — Normal Power Down Sequence with VR Disable Command

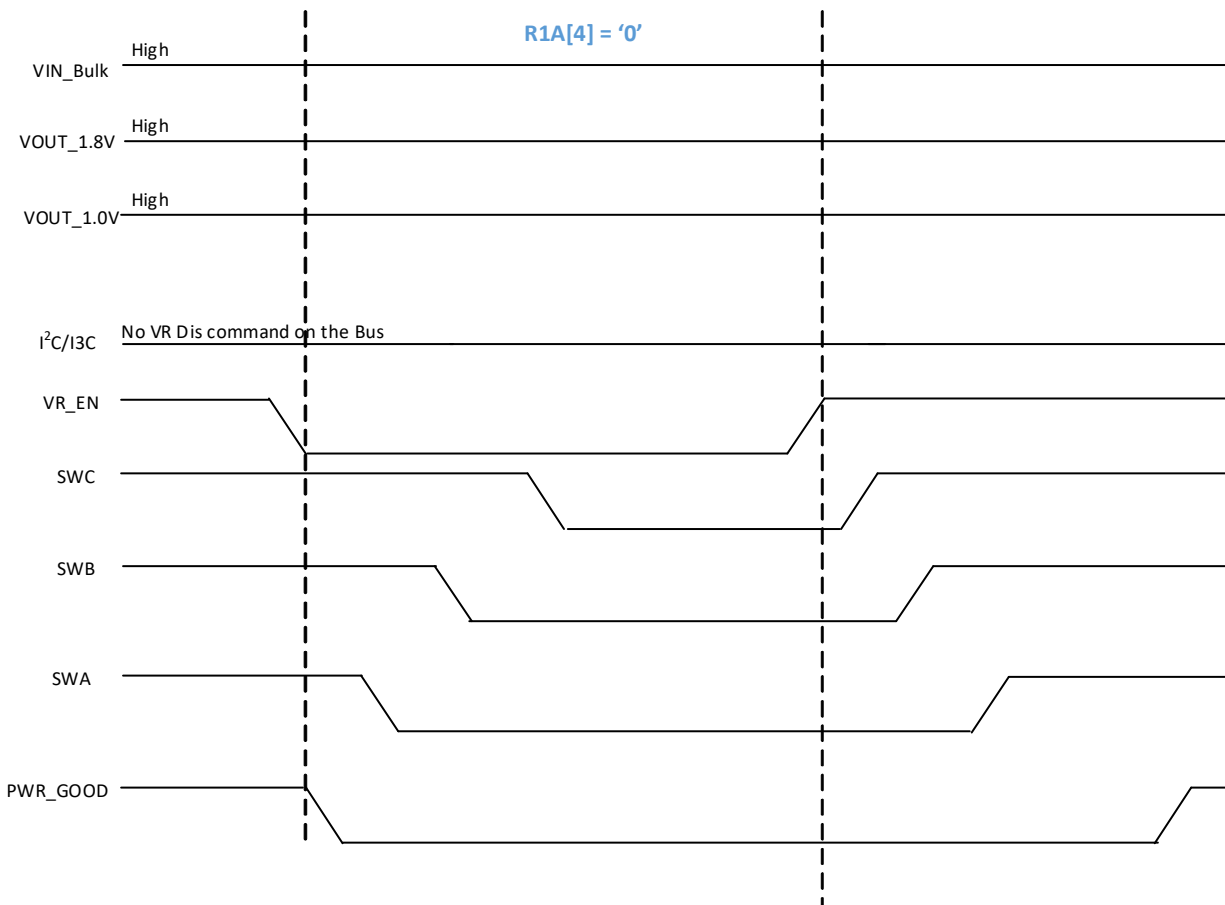
#### 4.6.2 Programmable Mode Operation; R1A[4] = '0'

The PMIC allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command ([Table 154, Register 0x32](#) [7] = '0' or VR\_EN pin transitions to low). The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers. The PMIC controls the PWR\_GOOD signal as following in bullet a and bullet b:
  - a. If VR Disable command with a pin (i.e., VR\_EN pin transitions to Low), PMIC asserts PWR\_GOOD signal Low. The host can re-enable the PMIC's output regulators by VR\_EN pin transition to High. The PMIC executes power on sequence config 0 to power on sequence config 3 registers and floats PWR\_GOOD signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. See [Figure 21](#). The PMIC does not require power cycle.
  - b. If VR Disable command on a I<sup>2</sup>C/I<sup>3</sup>C Bus (i.e., [Table 154, Register 0x32](#) [7] = '0'), PMIC keeps the PWR\_GOOD signal floating because this is an intentional command from the host and not a fault condition. The host can re-enable the PMIC's output regulators by issuing VR\_EN command on the I<sup>2</sup>C/I<sup>3</sup>C bus (i.e., [Table 154, Register 0x32](#) [7] = '1'). The PMIC executes power on sequence config 0 to power on sequence config 3 registers and continues to float the PWR\_GOOD signal until tPMIC\_PWR\_GOOD\_OUT time at which point, PMIC assumes normal control of PWR\_GOOD signal. See [Figure 22](#). The PMIC does not require power cycle.
  - c. The simultaneous usage of VR\_EN pin and I<sup>2</sup>C/I<sup>3</sup>C bus command to turn on/off the PMIC is not allowed. If the VR\_EN pin transitions to Low first, the PWR\_GOOD signal follows as described in bullet a and PWR\_GOOD signal remains low even if there is a subsequent I<sup>2</sup>C/I<sup>3</sup>C bus command as described in bullet b.
2. Configuring one or more bits in [Table 151, Register 0x2F](#) [6:3] to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) on its own. The PMIC keeps the PWR\_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in [Table 151, Register 0x2F](#) [6:3] to '1' in any specific sequence that is desired by the host. The PMIC keeps the PWR\_GOOD signal floating. The PWR\_GOOD signal behavior is same as in [Figure 22](#).
3. If [Table 154, Register 0x32](#) [5] = '1', driving PWR\_GOOD input low. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers and drives PWR\_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. If host re-enables PMIC's output regulators by issuing VR\_EN command on the I<sup>2</sup>C/I<sup>3</sup>C Basic bus (i.e., [Table 154, Register 0x32](#) [7] = '1'), the PMIC executes power on sequence config 0 to power on sequence config 2 registers and floats PWR\_GOOD output signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. The PMIC does not require power cycle.

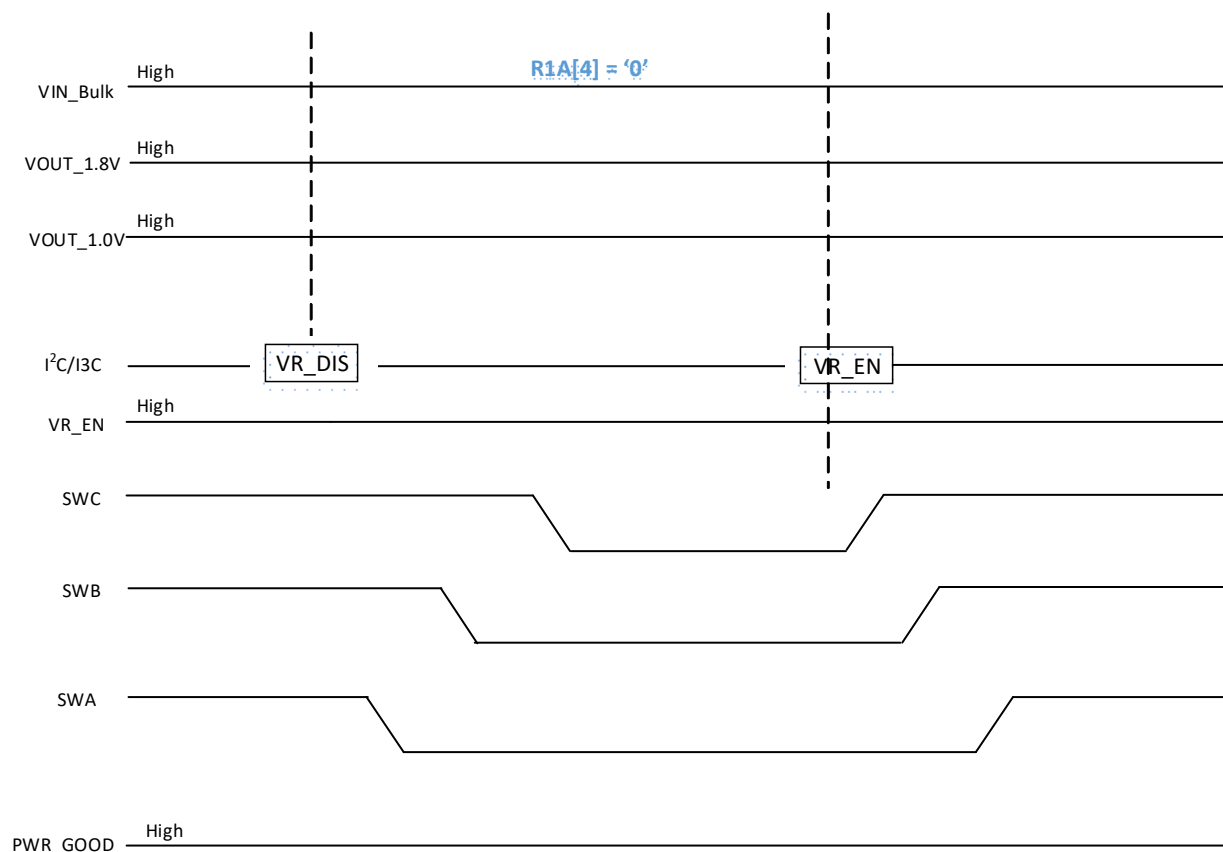
#### 4.6.2 Programmable Mode Operation; R1A[4] = '0' (cont'd)

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in [Table 27](#) under column “Trigger VR Disable”. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers. The PMIC asserts PWR\_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either [Table 154, Register 0x32 \[7\] = '1'](#) or VR\_EN pin transitions to high and PMIC turns on its output regulators and floats PWR\_GOOD signal. The PMIC does not require power cycle.



**Figure 21 — Power Down with VR\_EN Pin; R1A[4]=0; Program. Mode; PWR\_GOOD Signal**

#### 4.6.2 Programmable Mode Operation; R1A[4] = '0' (cont'd)



**Figure 22 — Power Down with VR\_DIS; R1A[4]=0; Program. Mode; PWR\_GOOD Signal**

#### 4.6.3 Programmable Mode Operation; R1A[4] = '1'

The PMIC allows host to power down any or all output regulators by any of the three methods below.

1. The VR Disable command (Table 154, Register 0x32 [7] = '0' or VR\_EN pin transitions to low). The PMIC executes power off sequence config0 (Table 200, Register 0x58) to power off sequence config3 (Table 203, Register 0x5B) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The PMIC retains the Table 152, Register 0x30 [2] value when entering in P1 state and restores the setting when it exits the P1 state. The PMIC controls the PWR\_GOOD signal as follows in bullet a and bullet b:
  - a. If VR Disable command with a pin (i.e., VR\_EN pin transitions to Low), PMIC asserts PWR\_GOOD signal Low. The host can re-enable the PMIC's output regulators by VR\_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config 0 to power on sequence config 2 registers and floats PWR\_GOOD signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. See Figure 23. The PMIC does not require power cycle.

#### 4.6.3 Programmable Mode Operation; R1A[4] = '1' (cont'd)

- b. If VR Disable command on a I<sup>2</sup>C/I<sup>3</sup>C Basic Bus (i.e., [Table 154, Register 0x32 \[7\] = '0'](#)), PMIC keeps the PWR\_GOOD signal floating because this is an intentional command from the host and not a fault condition. The PMIC exits from P1 state with only VR\_EN pin transition to High. The host can re-enable the PMIC's output regulators by VR\_EN pin transition to High and PMIC executes power on sequence config 0 to power on sequence config 3 registers. The PMIC continues to float PWR\_GOOD signal until tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied and at that point PMIC assumes normal control of PWR\_GOOD signal. See [Figure 24](#). The PMIC does not require power cycle.
    - c. The simultaneous usage of VR\_EN pin and I<sup>2</sup>C/I<sup>3</sup>C bus command to turn on/off the PMIC is not allowed. If the VR\_EN pin transitions to Low first, the PWR\_GOOD signal follows as described in bullet a and PWR\_GOOD signal remains low even if there is a subsequent I<sup>2</sup>C/I<sup>3</sup>C bus command as described in bullet b.
  2. Configuring one or more bits in [Table 151, Register 0x2F \[6:3\]](#) to '0' in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) on its own. The PMIC keeps the PWR\_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in [Table 151, Register 0x2F \[6:3\]](#) to '1' in any specific sequence that is desired by the host. The PMIC keeps the PWR\_GOOD signal floating. The PWR\_GOOD signal behavior is same as in [Figure 24](#).
  3. If [Table 154, Register 0x32 \[5\] = '1'](#), driving PWR\_GOOD input low. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers and drives PWR\_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. The PMIC does not enter in P1 state. If host re-enables PMIC's output regulators by issuing VR\_EN command on I<sup>2</sup>C/I<sup>3</sup>C Basic bus (i.e., [Table 154, Register 0x32 \[7\] = '1'](#)), the PMIC executes power on sequence config 0 to power on sequence config 3 registers and floats PWR\_GOOD signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in [Table 27](#) under column "Trigger VR Disable". The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR\_GOOD signal low. The host can re-enable PMIC's output regulators with VR Enable command with either [Table 154, Register 0x32 \[7\] = '1'](#) or VR\_EN pin transitions to high and PMIC turns on its output regulators and floats PWR\_GOOD signal. The PMIC does not require power cycle.

#### 4.6.3 Programmable Mode Operation; R1A[4] = '1' (cont'd)

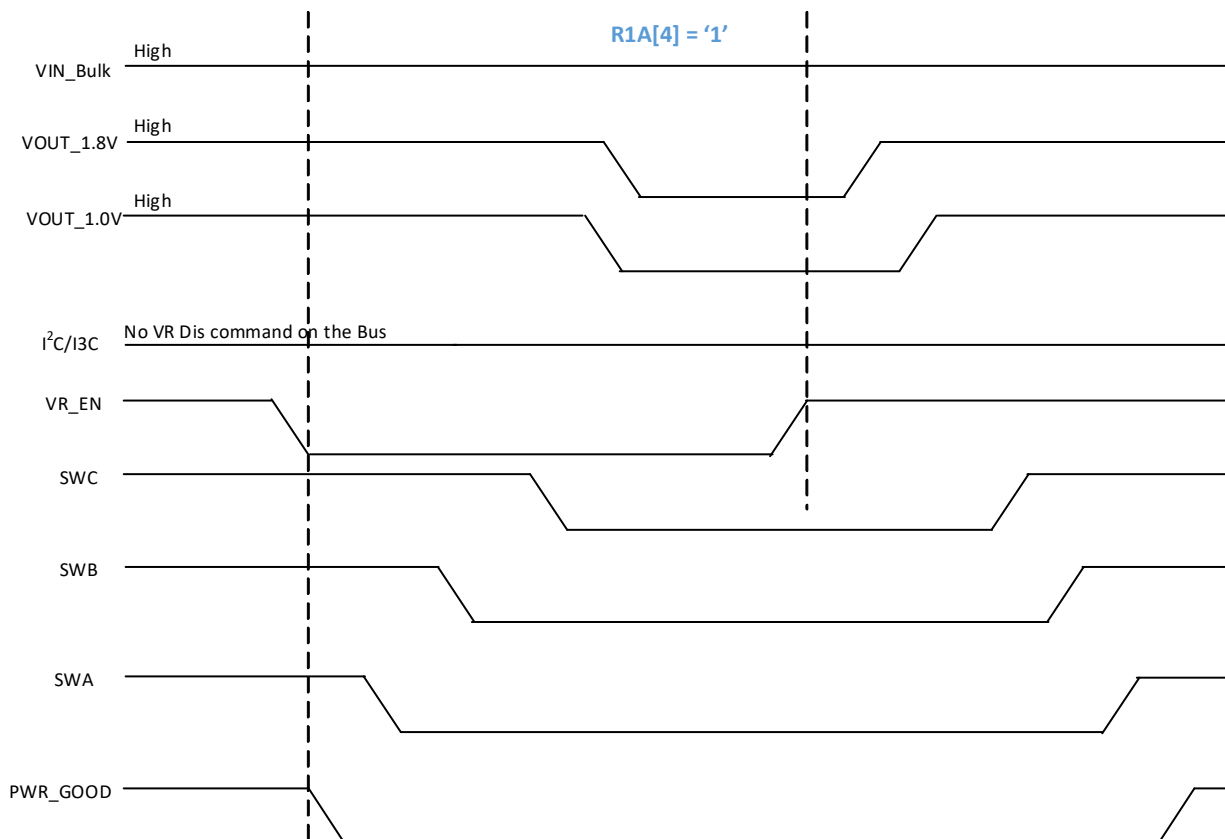


Figure 23 — Power Down with VR\_EN Pin; R1A[4]=1; Program. Mode; PWR\_GOOD Signal

### 4.6.3 Programmable Mode Operation; R1A[4] = '1' (cont'd)

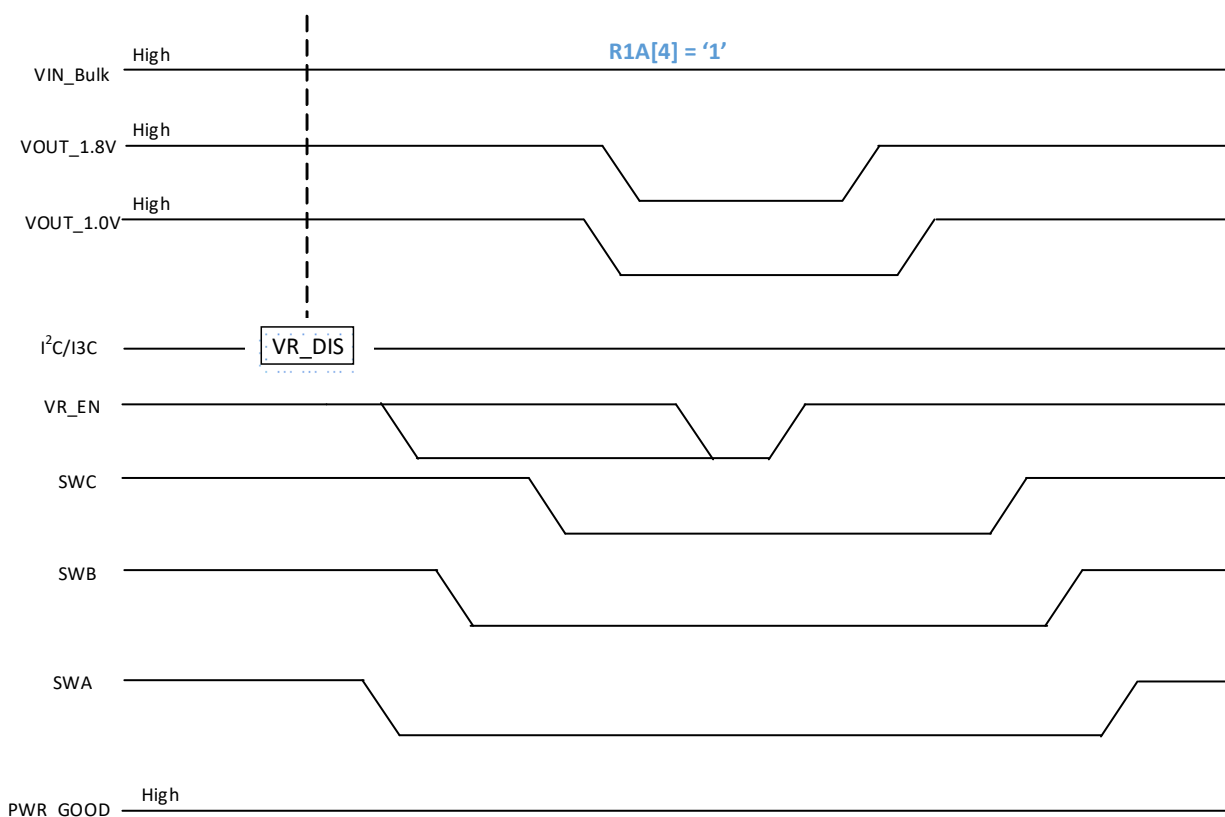


Figure 24 — Power Down with VR\_DIS; R1A[4]=1; Program. Mode; PWR\_GOOD Signal

### 4.6.4 Secure Mode Operation; R1A[4] = '0'

The PMIC allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR\_EN pin transitions to low. The PMIC asserts PWR\_GOOD signal Low. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers. The host can re-enable the PMIC's output regulators by VR\_EN pin transition to High. The PMIC executes power on sequence config 0 to power on sequence config 3 registers and floats PWR\_GOOD signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. See Figure 25. The PMIC does not require power cycle.
  - a. Note that VR Disable or Enable command on a I2C/I3C Basic Bus (i.e., [Table 154, Register 0x32](#) [7] = '0' or '1') has no effect on the PMIC. Also, configuring one or more bits in [Table 151, Register 0x2F](#) [6:3] to '0' has no effect on the PMIC. See [Figure 26](#).

#### 4.6.4 Secure Mode Operation; R1A[4] = '0' (cont'd)

2. If [Table 154, Register 0x32](#) [5] = '1', driving PWR\_GOOD input low. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers; drives PWR\_GOOD signal low and unlocks only [Table 154, Register 0x32](#) [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the [Table 154, Register 0x32](#) [7]. When host issues VR Enable command by I2C/I3C Basic bus, the PMIC executes Power on sequence config 0 to Power on sequence config 2 registers, floats PWR\_GOOD output signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied and re-locks register [Table 154, Register 0x32](#) [7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in [Table 27](#) under column "Trigger VR Disable". The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers. The PMIC asserts PWR\_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either [Table 154, Register 0x32](#) [7] = '1' or VR\_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR\_GOOD signal low.

#### 4.6.5 Secure Mode Operation; R1A[4] = '1'

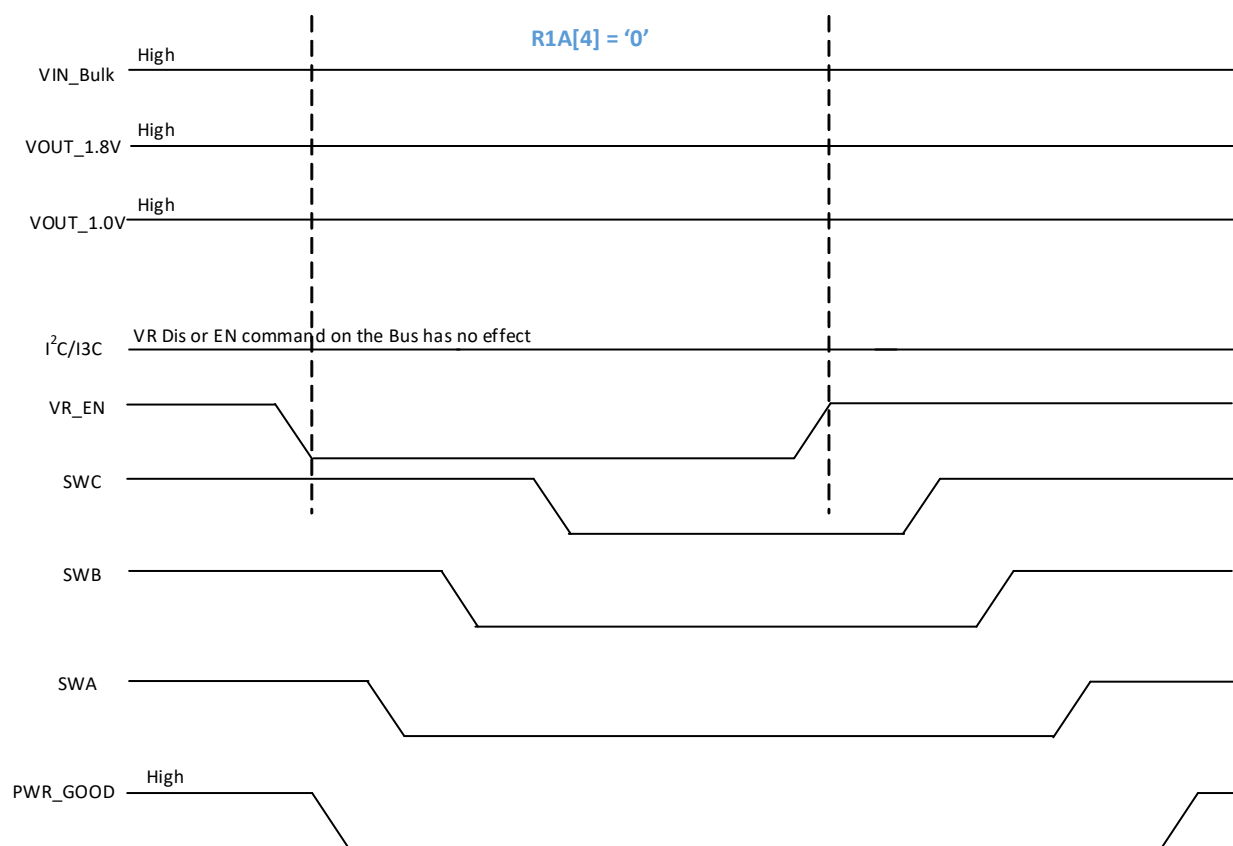
The PMIC allows host to power down any or all output regulators by any of the two methods below.

1. The VR Disable command with VR\_EN pin transitions to low. The PMIC asserts PWR\_GOOD signal Low. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The PMIC retains the [Table 152, Register 0x30](#) [2] value when entering in P1 state and restores the setting when it exits the P1 state. The host can re-enable the PMIC's output regulators by VR\_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config 0 to config 3 registers and floats PWR\_GOOD signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. See [Figure 27](#). The PMIC does not require power cycle.
  - a. Note that VR Disable or Enable command on a I2C/I3C Basic Bus (i.e., [Table 154, Register 0x32](#) [7] = '0' or '1') has no effect on the PMIC. Also, configuring one or more bits in [Table 151, Register 0x2F](#) [6:3] to '0' has no effect on the PMIC. See [Figure 26](#).
2. If [Table 154, Register 0x32](#) [5] = '1', driving PWR\_GOOD input low. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers; drives PWR\_GOOD signal low and unlocks only [Table 154, Register 0x32](#) [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write-protected registers locked except for the [Table 154, Register 0x32](#) [7]. The PMIC does not enter in P1 state. When host issues VR Enable command by I2C/I3C Basic bus, the PMIC executes Power on sequence config 0 to Power on sequence config 3 registers, floats PWR\_GOOD output signal after tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied and re-locks register [Table 154, Register 0x32](#) [7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.



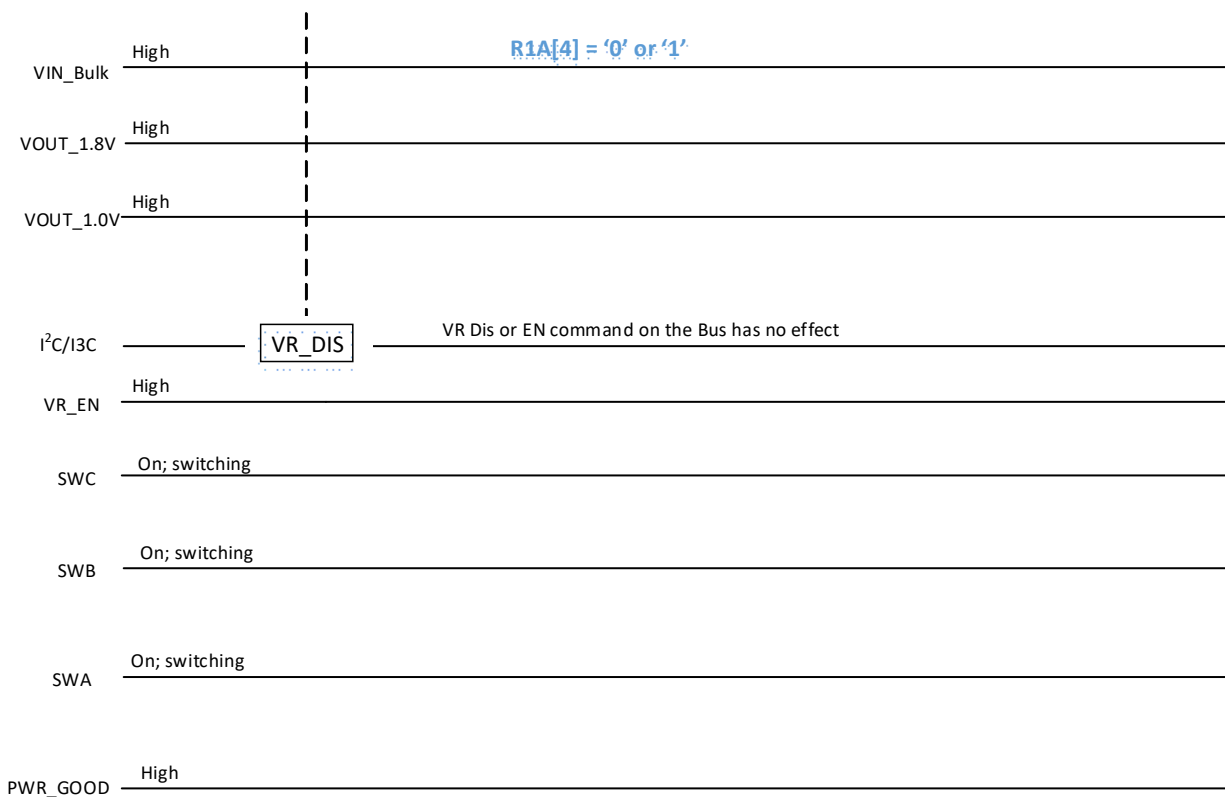
#### 4.6.5 Secure Mode Operation; R1A[4] = '1' (cont'd)

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in [Table 27](#) under column “Trigger VR Disable”. The PMIC executes power off sequence config0 ([Table 200, Register 0x58](#)) to power off sequence config3 ([Table 203, Register 0x5B](#)) to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR\_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either [Table 154, Register 0x32](#) [7] = '1' or VR\_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR\_GOOD signal low.



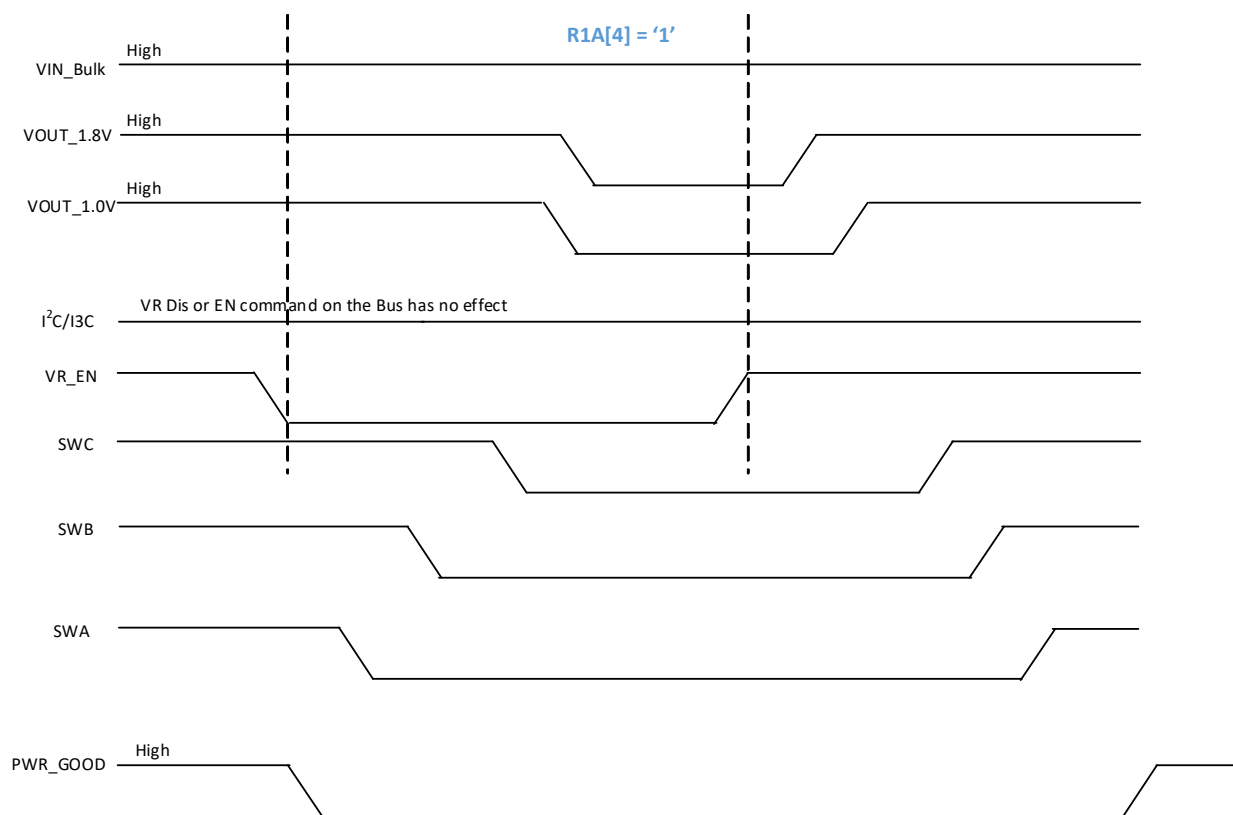
**Figure 25 — Power Down with VR\_EN Pin; R1A[4]=0; Secure Mode; PWR\_GOOD Signal**

#### 4.6.5 Secure Mode Operation; R1A[4] = '1' (cont'd)



**Figure 26 — VR\_DIS or VR\_EN CMD on Bus; R1A[4]=x; Secure Mode; PWR\_GOOD Signal**

#### 4.6.5 Secure Mode Operation; R1A[4] = '1' (cont'd)



**Figure 27 — Power Down with VR\_EN Pin; R1A[4]=1; Secure Mode; PWR\_GOOD Signal**

#### 4.7 PMIC Output Rail Off Timing Due to Fault Event

Figure 28 shows the timing relationship once the PMIC registers VR Disable command internally due to fault condition on SWA output as listed in [Table 27, Events Interrupt Summary](#). The waveform shows each buck regulator output soft stop time and delay time once the soft stop time expires from each power off sequence config0 to power off sequence config3 registers. Note that, if more than one regulator is disabled in a power off sequence config register and if those regulators have different soft stop time programmed, then the larger value of that soft stop time is used as a reference for delay timer to start. Each regulator will still follow different soft stop time to turn off the buck regulator.

The specific example in [Figure 28](#) uses four power off sequence config0 to config3 registers and only one buck regulator is disabled in each power off sequence config 0, config 1, config 2, and config 3 registers.

## 4.7 PMIC Output Rail Off Timing Due to Fault Event (cont'd)

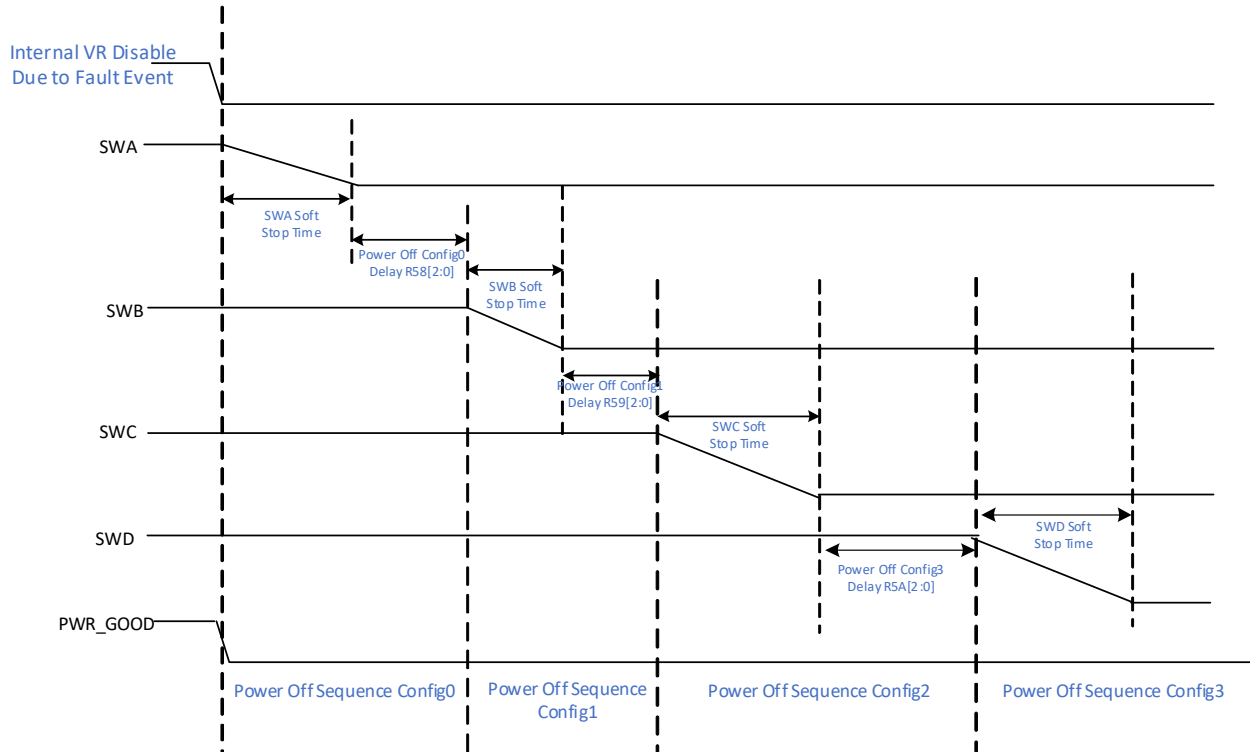


Figure 28 — PMIC Power Off Timing Due to Internal Fault Condition

### 4.7.1 Power Down Output Regulators During Power On Sequence

During power on as described in Clause 4.2, it is possible that PMIC can trigger VR Disable command on its own as described in [Table 27, Events Interrupt Summary](#) when one or more regulators are already turned on even while other remaining output regulators are not yet turned on because PMIC has not completed the power on sequence config registers. For these types of cases, the PMIC will not execute the remaining power on sequence config registers and will immediately jump to executing the power off sequence config0 to power off sequence config3 registers. The PMIC will update the status registers and error log registers appropriately as normal because it generated VR Disable command on its own. The PWR\_GOOD output signal would remain low.

## 4.8 Power Good (PWR\_GOOD) Signal

The PWR\_GOOD output signal type can be configured as either output only or input and output through register [Table 154, Register 0x32](#) [5]. By default, PWR\_GOOD is an output signal. The PWR\_GOOD signal can only be configured once, at power on, before issuing VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus). The PWR\_GOOD signal configuration applies to both secure mode and programmable mode of operation.

Clause [4.8.1](#), clause [4.8.2](#), [Table 23](#), and [Table 24](#) describe PMIC behavior.

## 4.8 Power Good (PWR\_GOOD) Signal (cont'd)

**Table 23 — PMIC Operation; PWR\_GOOD Type: Input and Output**

External PWR_GOOD Input	PMIC's Internal PWR_GOOD	PMIC Operation	Notes
High	High	High (Power Good) Normal Operation	
High	Low	Low (Power Not Good) PMIC Communicates its Status; clause 4.8.1	[1],[2]
Transition from High to Low	High	Low; (PMIC Good) PMIC Executes VR Disable Command	[3]
Low	Low	Low; (PMIC Power Not Good) PMIC Internally Generates VR Disable Command	

NOTE 1 The PMIC indicates its own internal status and it may shut down on its own by following Power Off Config0 to Power Off config3 sequence.

NOTE 2 This is a transient state and the net results of the PWR\_GOOD signal is Low.

NOTE 3 The PMIC shuts down based on external command by following Power Off Config0 to Power Off config3 sequence.

**Table 24 — PMIC Operation; PWR\_GOOD Type: Output Only**

External PWR_GOOD Input	PMIC's Internal PWR_GOOD	PMIC Operation	Notes
X (High or Low)	High	Normal Operation	
X (High or Low)	Low	PMIC communicates its status; clause 4.8.1	[1]

NOTE 1 The PMIC indicates its own internal status and it may shut down on its own by following Power Off Config0 to Power Off config3 sequence.

### 4.8.1 PWR\_GOOD as Output Only Signal

When [Table 154, Register 0x32](#) [5] = '0', the PWR\_GOOD signal type is output only; the input of PWR\_GOOD signal is ignored.

The PMIC PWR\_GOOD pin indicates status of VIN\_Bulk input supply and all output regulators (VOUT\_A, VOUT\_B, VOUT\_C, VOUT\_1.8V, and VOUT\_1.0V). The PMIC floats PWR\_GOOD pin when VIN\_Bulk input supply is valid and all enabled output regulator's (VOUT\_A, VOUT\_B, VOUT\_C, VOUT\_1.8V, and VOUT\_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power up, when input supply VIN\_Bulk is ramped up and stable, the PMIC keeps PWR\_GOOD pin asserted to low; however PMIC updates corresponding status register. By default, the register [Table 154, Register 0x32](#) [5] = '0'. Once PMIC receives VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus) from the host, the PMIC enables all appropriate output regulators and updates corresponding status registers and enters into operating state called "Regulation". At this point, PMIC floats PWR\_GOOD pin and the external board pullup resistor pulls the pin high as there may be other PMIC on different CAMM2 may be driving the PWR\_GOOD pin low. Once the PWR\_GOOD pin is pulled high (i.e., no other PMIC is driving the PWR\_GOOD pin low), the PMIC remains in "Regulation" state.

#### 4.8.1 PWR\_GOOD as Output Only Signal (cont'd)

Once the PWR\_GOOD pin is high, if PMIC detects any condition either on VIN\_Bulk input supply or any of the output regulators (VOUT\_A, VOUT\_B, VOUT\_C, VOUT\_1.8V, and VOUT\_1.0V) that causes the PMIC to update its status registers to indicate the power status is not good, then PMIC asserts PWR\_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR\_GOOD pin float (i.e., get High) even if the condition that triggered the PMIC to assert the PWR\_GOOD pin no longer exists. In other words, the PMIC's PWR\_GOOD pin is latched and, once latched, it must be explicitly addressed by the host.

If PMIC is operating in Secure mode of operation, see clause 4.6.4 and clause 4.6.5 for additional information.

If PMIC is in Programmable mode of operation, see clause 4.6.2 and clause 4.6.3 for additional information.

#### 4.8.2 PWR\_GOOD as Input and Output Signal

When Table 154, Register 0x32 [5] = '1', the PWR\_GOOD signal type is both input and output and is only applicable after host issues VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C Basic bus). Also note that simultaneous usage of PWR\_GOOD pin as IO and VR\_EN pin is not allowed and considered an illegal configuration. In other words, if VR\_EN pin is intended to be used to turn on and turn off output rails, the PWR\_GOOD pin must be configured as output only. If PWR\_GOOD pin is intended to be used as IO, the VR\_EN pin must be connected to GND on the board.

The PMIC PWR\_GOOD pin indicates status of VIN\_Bulk input supply and all output regulators (VOUT\_A, VOUT\_B, VOUT\_C, VOUT\_1.8V, and VOUT\_1.0V). The PMIC floats PWR\_GOOD pin when VIN\_Bulk input supply is valid and all enabled output regulator's (VOUT\_A, VOUT\_B, VOUT\_C, VOUT\_1.8V, and VOUT\_1.0V) tolerances are maintained as configured in the appropriate register space.

At first power up, when input supply VIN\_Bulk is ramped up and stable, the PMIC keeps PWR\_GOOD pin asserted to low; however PMIC updates corresponding status register. The host, prior to issuing VR Enable command on I<sup>2</sup>C/I<sup>3</sup>C Basic bus, can configure the register Table 154, Register 0x32 [5] = '1'. When host issues VR Enable command on I<sup>2</sup>C/I<sup>3</sup>C Basic bus, the PMIC turns on its output regulators and updates corresponding status registers and enters into operating state called "Regulation". At this point, the PMIC floats PWR\_GOOD pin and waits for external board pullup resistor to pull the pin high as there may be other PMIC on different CAMM2 may be driving the PWR\_GOOD pin low. Once the PWR\_GOOD pin is pulled high (i.e., no other PMIC is driving the PWR\_GOOD pin low), the PMIC automatically enters in to operating state called "Bulk Control Link Monitor".

Once the PWR\_GOOD pin is high, if PMIC detects any condition either on VIN\_Bulk input supply or any of the output regulators (VOUT\_A, VOUT\_B, VOUT\_C, VOUT\_1.8V, and VOUT\_1.0V) that causes the PMIC to update its status registers to indicate the power status is not good, then PMIC asserts PWR\_GOOD pin low and keeps it asserted until the host explicitly takes a specific action corresponding to it. The PMIC does not automatically let the PWR\_GOOD pin float (i.e., get High) even if the condition that triggered the PMIC to assert the PWR\_GOOD pin no longer exists. In other words, the PMIC's PWR\_GOOD pin is latched and once latched, it must be explicitly addressed by the host.

In this "Bulk Control Link Monitor" operating state, the PMIC behavior is as follows:

If PMIC is operating in Secure mode of operation, see clause 4.6.4 and clause 4.6.5 for additional information.

#### 4.8.2 PWR\_GOOD as Input and Output Signal (cont'd)

- PMIC allows PWR\_GOOD input signal low at any time. The host must keep the PWR\_GOOD signal low for minimum tPWR\_GOOD\_Low\_Pulse\_Width to issue command to PMIC to execute VR Disable. When PMIC detects PWR\_GOOD signal low, the PMIC internally triggers VR Disable command and shuts off all output regulators (the PMIC executes power off sequence config0 (Table 200, Register 0x58) to power off sequence config3 (Table 203, Register 0x5B)); drives PWR\_GOOD signal low and unlocks only Table 154, Register 0x32 [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the Table 154, Register 0x32 [7]. As long as there is valid VIN\_Bulk input supply, the PMIC allows read access to all its configuration registers. The PMIC allows write access to non-locked configuration registers and register Table 154, Register 0x32 [7]. If host issues VR Enable command by I<sup>2</sup>C/I<sup>3</sup>C bus, the PMIC executes Power on sequence config 0 to Power on sequence config 3 registers, floats PWR\_GOOD output signal and re-locks register Table 154, Register 0x32 [7].

If PMIC is in Programmable mode of operation, see clause 4.6.2 and clause 4.6.3 for additional information.

- PMIC allows PWR\_GOOD input signal low at any time. The host must keep the PWR\_GOOD signal low for minimum tPWR\_GOOD\_Low\_Pulse\_Width to issue command to PMIC to execute VR Disable. When PMIC detects PWR\_GOOD signal low, the PMIC internally triggers VR Disable command and shuts off all output regulators (the PMIC executes power off sequence config0 (Table 200, Register 0x58) to power off sequence config3 (Table 203, Register 0x5B)); drives PWR\_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. As long as there is valid VIN\_Bulk input supply, the PMIC allows read and write access to all its configuration registers. The host can issue VR Enable command with VR\_EN command on I<sup>2</sup>C/I<sup>3</sup>C Basic bus (i.e., Table 154, Register 0x32 [7] = '1') again to turn on the PMIC's output regulator and PMIC will execute Power On Config0 to Config3 registers and floats PWR\_GOOD output signal.

#### 4.9 Idle Condition and Quiescent Power State

Quiescent Power State definition: All circuits including PMIC switch output and LDO output regulators are off. VR\_EN signal is at static low or high level. I<sup>2</sup>C or I<sup>3</sup>C Basic interface access is not allowed and is pulled high. PID signal is at static low or high level. Unlock input pin interface is turned off but the input pin level can be at static low or high. This state is only applicable if Table 130, Register 0x1A [4] = '1'. This state is labeled as P1 state in Figure 29.

Idle Condition definition: All circuits including PMIC switch output and LDO output regulators are on with 0 A load. VR\_EN signal is at static low or high level. I<sup>2</sup>C or I<sup>3</sup>C Basic interface access is allowed but bus is pulled high. PID signal is at static low or high level. Unlock input pin is at static low or high level.

Figure 29 shows high level PMIC states and its definition. The state transitions from each state is defined in Table 25.

## 4.9 Idle Condition and Quiescent Power State (cont'd)

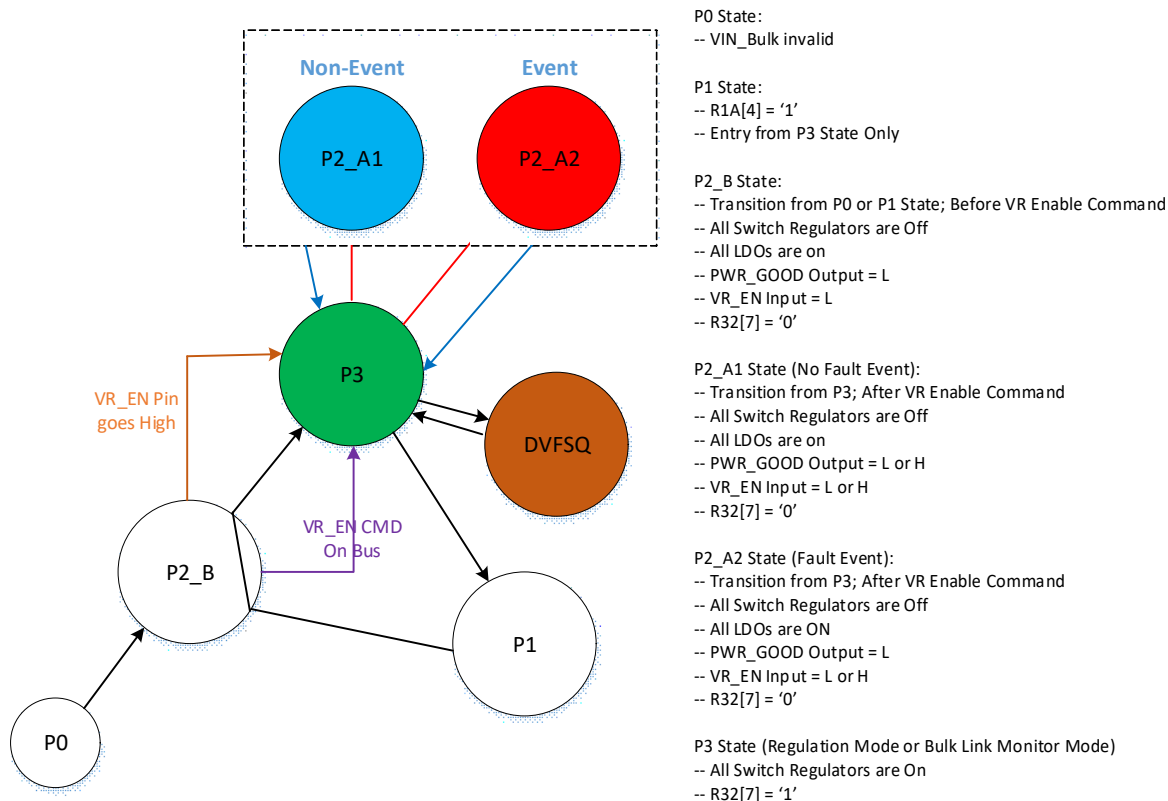


Figure 29 — State Definition and Transitions

Table 25 — State Transitions

Start State	Activity	Register Setting				End State	PWR_GOOD Output <sup>[1]</sup>	Power Cycle Required?	Note
		R2F[2]	R32[5]	R1A[4]	R2E[4]				
P0	Valid VIN_Bulk	N/A	N/A	N/A	N/A	P2_B	Low	N/A	
P1	VR_EN; High to Low	X	X	X	X	N/A			
	VR_EN Pin; Low to High	X	X	0	X	N/A			
		X	X	1	X	P3	Hi-Z	No	
	VR_DIS CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	X	X	1	X	P1	No Change	N/A	
	VR_EN CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	X	X	1	X	P1	No Change	N/A	
	DVFSQ_n; High to Low	X	X	X	X	Illegal for system; PMIC ignores it			
P2_B	VR_EN Pin Transition to High	X	0	X	X	P3	Hi-Z	N/A	
		X	1	X	X	Illegal Configuration			2
	VR_EN CMD on Bus	X	X	X	X	P3	Hi-Z	N/A	
	DVFSQ_n; High to Low	X	X	X	X	Illegal for system; PMIC ignores it			
	DVFSQ_n; Low to High	X	X	X	X	P2_B	No Change	N/A	



Table 25 — State Transitions (cont'd)

Start State	Activity	Register Setting				End State	PWR_GOOD Output <sup>[1]</sup>	Power Cycle Required?	Note
		R2F[2]	R32[5]	R1A[4]	R2E[4]				
P3	VR_EN Pin; High to Low	X	0	0	X	P2_A1	Low		
		X	0	1	X	P1	Low		
		X	1	X	X	Illegal Configuration			[2]
	VR_EN Pin; Low to High	X	X	X	X	P3	Hi-Z	N/A	[3]
	VR_DIS CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	1	X	0	X	P2_A1	Hi-Z		
		1	X	1	X	P1	Hi-Z		
		0	X	X	X	P3	Hi-Z	N/A	
	VR_EN CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	X	X	X	X	P3	Hi-Z	N/A	[4]
	PWR_GOOD Input Low	X	0	X	X	P3	Hi-Z	N/A	[5],[6]
		1	1	X	X	P2_A1	Low		6
		0	1	X	X	P2_A1	Low		6
	Internal VR Disable Event	0	X	X	X	P2_A2	Low	Yes	
		1	X	X	X	P2_A2	Low	No	[7]
	VIN_Bulk Invalid	X	X	X	X	P0	N/A	N/A	
	DVFSQ_n High to Low	X	X	X	0	No Change		N/A	
		X	X	X	1	DVFSQ	No Change	N/A	
	DVFSQ_n Low to High	X	X	X	X	No Change	No Change	N/A	
P2_A1	VR_EN Pin; High to Low	X	X	X	X	No Change	No Change	N/A	[8]
	VR_EN Pin; Low to High	X	1	X	X	Illegal Configuration			2
		X	0	0	X	P3	Hi-Z	No	
		X	0	1	X	N/A			[9]
	VR_DIS CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	X	X	X	X	No Change	No Change	N/A	[10]
	VR_EN CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	0	0	0	X	No Change	No Change	N/A	
		0	1	X	X	P3	Hi-Z	No	
		0	0	1	X	N/A	N/A	N/A	
		1	X	0	X	P3	Hi-Z	No	
		1	1	1	X	P3	Hi-Z	No	
		1	0	1	X	N/A			8
	Internal VR Disable Event	0	X	X	X	P2_A2	Low	Yes	
		1	X	X	X	P2_A2	Low	No	7,[11]
	VIN_Bulk Invalid	X	X	X	X	P0	N/A	N/A	
	DVFSQ_n High to Low	X	X	X	X	Illegal Configuration			
	DVFSQ_n Low to High	X	X	X	X	P2_A1	No Change	N/A	
P2_A2	VR_EN Pin; High to Low	X	X	X	X	No Change	No Change	N/A	[12]
	VR_EN Pin; Low to High	0	X	X	X	P2_A2	Low	Yes	
		1	0	0	X	P3	Hi-Z	No	
		1	0	1	X	P3	Hi-Z	No	
		1	1	X	X	Illegal Configuration			2
	VR_EN CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	0	X	X	X	P2_A2	Low	Yes	
		1	X	0	X	P3	Hi-Z	No	
		1	0	1	X	P3	Hi-Z	No	
		1	1	1	X	P3	Hi-Z	No	
	Internal VR Disable Event	0	X	X	X	No Change	No Change	Yes	
		1	X	X	X	No Change	No Change	No	7,11
	VIN_Bulk Invalid	X	X	X	X	P0	N/A	N/A	
	DVFSQ_n High to Low	X	X	X	X	Illegal Configuration			
	DVFSQ_n Low to High	X	X	X	X	P2_A2	No Change	N/A	

Table 25 — State Transitions (cont'd)

Start State	Activity	Register Setting				End State	PWR_GOOD Output <sup>[1]</sup>	Power Cycle Required?	Note
		R2F[2]	R32[5]	R1A[4]	R2E[4]				
DVFSQ	VR_EN Pin High to Low	X	0	0	1	P2_A1	Low		
		X	0	1	1	P1	Low		
		X	1	X	X	Illegal Configuration			2
	VR_EN Pin Low to High	X	X	X	1	DVFSQ	Hi-Z	N/A	3
	VR_DIS CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	1	X	0	1	P2_A1	Hi-Z		
		1	X	1	1	P1	Hi-Z		
		0	X	X	1	DVFSQ	Hi-Z	N/A	
	VR_EN CMD on I <sup>2</sup> C/I <sup>3</sup> C Bus	X	X	X	1	DVFSQ	Hi-Z	N/A	4
	PWR_GOOD Input Low	X	0	X	1	DVFSQ	Hi-Z	N/A	5,6
		1	1	X	1	P2_A1	Low		6
		0	1	X	1	P2_A1	Low		6
	Internal VR Disable Event	0	X	X	1	P2_A2	Low	Yes	
		1	X	X	1	P2_A2	Low	No	7
	VIN_Bulk Invalid	X	X	X	X	P0	N/A	N/A	
	DVFSQ_n High to Low	X	X	X	0	N/A; Illegal Configuration			
		X	X	X	1	DVFSQ	No Change		[13]
	DVFSQ_n Low to High	X	X	X	0	N/A; Illegal Configuration			
		X	X	X	1	P3	No Change		

NOTE 1 This represents PMIC's PWR\_GOOD output signal; all power is good; no fault event.

NOTE 2 Simultaneous usage of VR\_EN pin and PWR\_GOOD IO type (Table 154, Register 0x32 [5] = '1') is not allowed and considered an illegal configuration. If VR\_EN pin is intended to be used to turn on or off output rails, PWR\_GOOD signal must be configured as O only (i.e., Table 154, Register 0x32 [5] = '0'). VR\_EN pin must be tied to GND if PWR\_GOOD signal is intended to be configured as IO (Table 154, Register 0x32 [5] = '1').

NOTE 3 PMIC is already in P3 state. It assumes PMIC entered in P3 state with VR\_EN command on I<sup>2</sup>C/I<sup>3</sup>C bus.

NOTE 4 PMIC is already in P3 state. It assumes PMIC entered in P3 state with VR\_EN pin transition to High.

NOTE 5 PMIC PWR\_GOOD IO Type is configured as Output Only.

NOTE 6 PMIC's input of PWR\_GOOD is Low. But internally, PMIC's PWR\_GOOD output signal is Hi-Z.

NOTE 7 PMIC allows to re-enable output regulators with VR Enable command (either with VR\_EN pin or on I<sup>2</sup>C/I<sup>3</sup>C bus) assuming that event is no longer present and status registers are cleared.

NOTE 8 PMIC is already in P2\_A1 state and so VR\_EN pin transition has no meaning.

NOTE 9 Since Table 130, Register 0x1A [4] = '1', the PMIC never enters into P2\_A1 state if there is no event, PMIC always enters in P1 state.

NOTE 10 PMIC is already in P2\_A1 state with VR\_EN pin. So VR\_DIS command on the bus has no effect.

NOTE 11 Power cycle is always required if there is a thermal shutdown regardless of the register Table 151, Register 0x2F [2] setting.

NOTE 12 PMIC is already in P2\_A2 state and so VR\_EN pin transition has no meaning.

NOTE 13 PMIC is already in DVFSQ state and hence DVFSQ\_n pin transition high to low has no meaning.

## 4.10 GSI\_n Pin Function

General Status Interrupt (GSI\_n) is an open drain output signal. By default at power on, GSI\_n output is disabled. The host can enable the GSI\_n output by setting Table 131, Register 0x1B [3] = '1'. Typically GSI\_n output is pulled up to 1 K $\Omega$  resistor to 1.8 V or 3.3 V. The PMIC asserts GSI\_n output for the event as described in Table 27.

## 4.11 Unlock Pin Function

Unlock is an asynchronous, active high, input signal. The voltage level on the Unlock input pin is identified in [Table 155, Register 0x33 \[0\]](#). By default at power on, the Unlock input pin function is enabled and the input receiver is active. The host can disable the Unlock input pin function by writing [Table 150, Register 0x2E \[3\]](#) = '0' when PMIC is in the P2\_B state prior to assertion of the first VR\_EN command (either by I<sup>2</sup>C/I<sup>3</sup>C bus or via VR\_EN input pin). The PMIC turns off the input receiver for Unlock pin when the input pin function is disabled.

After exiting the P2\_B power state, Unlock\_Pin\_Enable ([Table 150, Register 0x2E \[3\]](#)) can only be cleared by writing secure mode ([Table 151, Register 0x2F \[2\]](#)) = '0', which forces the PMIC to operate in the locked security states. The values of the registers [Table 150, Register 0x2E \[3\]](#), [Table 151, Register 0x2F \[2\]](#), and [Table 155, Register 0x33 \[0\]](#) define the register security state status as identified by the [Table 26](#) and [Figure 30](#). Sub-state transitions between P1, P2\_A1, P2\_A2, P3, and DVFSQ for each security state are defined by [Table 26](#) and [Figure 30](#).

If [Table 150, Register 0x2E \[3\]](#) = '0' in the P2\_B power state at the time VR\_EN command (either by I<sup>2</sup>C/I<sup>3</sup>C bus or VR\_EN input pin), the Unlock pin is disabled and register security is determined by the status of [Table 151, Register 0x2F \[2\]](#).

- If [Table 151, Register 0x2F \[2\]](#) = '0', the PMIC enters the locked security states and operates in secure mode. A power cycle is required to enable Unlocked or Configurable\_lock security states.
- If [Table 151, Register 0x2F \[2\]](#) = '1', the PMIC enters in the unlocked security states and operates in programmable mode. The PMIC transitions from unlocked to locked security states when [Table 151, Register 0x2F \[2\]](#) = '0' is written at which point PMIC disables the Unlock pin by setting [Table 150, Register 0x2E \[3\]](#) = '0' and places the registers in secure mode. A power cycle is required to enable Unlocked or Configurable\_lock security states.

When [Table 150, Register 0x2E \[3\]](#) = '1', the register [Table 151, Register 0x2F \[2\]](#) follows the input voltage level applied to the Unlock pin at the time or after VR\_EN command (either by I<sup>2</sup>C/I<sup>3</sup>C bus or VR\_EN input pin). Note that prior to first VR\_EN command (i.e., when PMIC is in P2\_B state), [Table 151, Register 0x2F \[2\]](#) does not follow the Unlock pin.

- When Unlock pin is high then [Table 155, Register 0x33 \[0\]](#) = '1' and [Table 151, Register 0x2F \[2\]](#) = '1'.
- When Unlock pin is low then [Table 155, Register 0x33 \[0\]](#) = '0' and [Table 151, Register 0x2F \[2\]](#) = '0'.

When [Table 150, Register 0x2E \[3\]](#) = '1', if Unlock pin is low in the P2\_B power state at the time VR\_EN command (either by I<sup>2</sup>C/I<sup>3</sup>C bus or VR\_EN input pin), the PMIC enters the locked security states with registers operating in secure mode, sets [Table 151, Register 0x2F \[2\]](#) = '0' and disables Unlock pin by setting [Table 150, Register 0x2E \[3\]](#) = '0'. A power cycle is required to enable Unlocked or Configurable\_lock security states.

## 4.11 Unlock Pin Function (cont'd)

When [Table 150, Register 0x2E](#) [3] = '1', if Unlock pin is high in the P2\_B power state at the time VR\_EN command (either by I<sup>2</sup>C/I<sup>3</sup>C bus or VR\_EN input pin), the PMIC enters Configurable lock security states where registers are in programmable mode when Unlock pin is high and in secure mode when Unlock pin is low. The PMIC transitions from configurable lock to locked security states when [Table 151, Register 0x2F](#) [2] = '0' is written at which point PMIC disables the Unlock pin by setting [Table 150, Register 0x2E](#) [3] = '0' and places the registers in secure mode. A power cycle is required to enable Unlocked or Configurable\_lock security states.

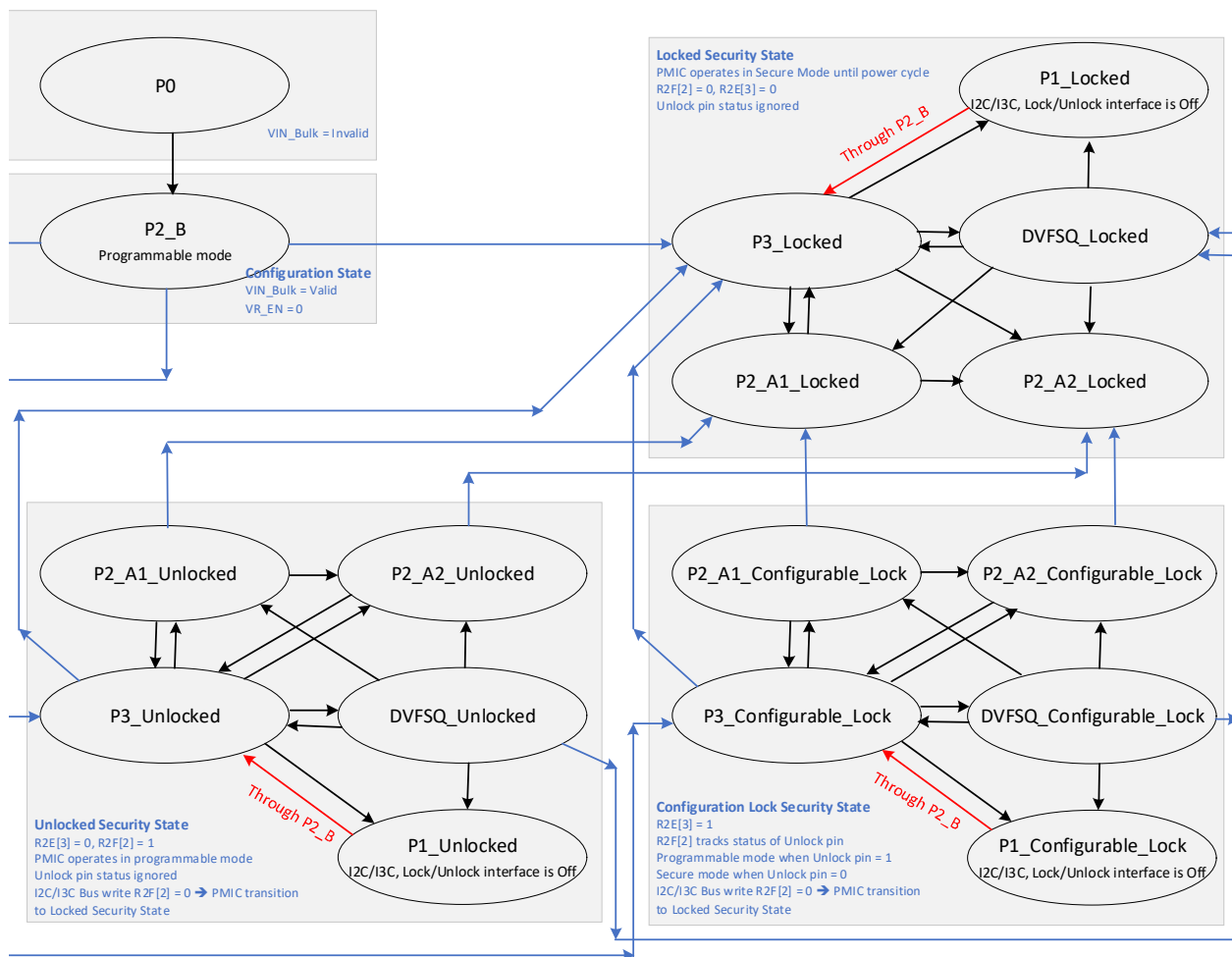


Figure 30 — Security State Flow Diagram

#### 4.11 Unlock Pin Function (cont'd)

Table 26 — PMIC Security State Transition

Start State					Event	End State				Notes
State	R2E[3]	Unlock Input Pin	R2F[2]	Register Status		State	R2E[3]	R2F[2]	Register Status	
P0	N/A	N/A	N/A	N/A	Valid VIN_Bulk	P2_B	1	0	Program mable	
P2_B	0	X	0	Program mable	VR_EN = 1	P3_Locked	0	0	Secure	[1]
			1			P3_Unlock ed	0	1	Program mable	[2]
	1	0	X	Program mable	VR_EN = 1 <sup>[3]</sup>	P3_Locked	0	0	Secure	[1],[4]
		1				P3_Configr able_Lock	1	1	Program mable	[5]
P3_Locked	0	X	0	Secure	Write to R2F[2] or R2E[3] is don't care	P3_Locked	0	0	Secure	
P3_Unlock ed	0	X	1	Program mable	Write R2F[2] = '0'	P3_Locked	0	0	Secure	
	0	X	1		Write R2E[3] = '0'	P3_Unlock ed	0	1	Program mable	[6]
P3_Configu rable_Lock	1	1	1	Program mable	Unlock --> Low	P3_Configu rable_Lock	1	0	Secure	
					Write R2E[3] = '0'		1	1	Program mable	[7]
					Write R2F[2] = '0'	P3_Locked	0	0	Secure	
	1	0	0	Secure	Unlock --> High	P3_Configu rable_Lock	1	1	Program mable	
					Write R2E[3] = '0'		1	0	Secure	[7]
P3_Unlock ed	0	X	1	Program mable	See Table 25	DVFSQ Unlocked	0	1	Program mable	
	0	X	1	Program mable	VR_EN --> Low	P2_A1_Unl ocked	0	1	Program mable	[8],[9]
					Write R32[7] = '0'					[8],[10]
					PWR_GOOD --> Low					[9],[11]
					Internal VR Disable Fault	P2_A2_Unl ocked	0	1	Program mable	[9],[11]
					VR_EN --> Low	P1_Unlock ed	0	1	N/A	[9],[12]
					Write R32[7] = '0'					[10],[12]

Table 26 — PMIC Security State Transition (cont'd)

Start State					Event	End State				Notes
State	R2E[3]	Unlock Input Pin	R2F[2]	Register Status		State	R2E[3]	R2F[2]	Register Status	
P3_Locked	0	X	0	Secure	See Table 25	DVFSQ Locked	0	0	Secure	
	0	X	0	Secure	VR_EN --> Low	P2_A1_Locked	0	0	Secure	[8],[9]
					PWR_GOOD --> Low					[9],[11]
					Internal VR Disable Fault	P2_A2_Locked	0	0	Secure	[9],[11]
					VR_EN --> Low	P1_Locked	0	0	N/A	[9],[12]
P3_Configurable_Lock	1	1	1	Programmable	See Table 25	DVFSQ Configurable Locked	1	1	Programmable	
	1	1	1	Programmable	VR_EN --> Low	P2_A1_Configurable_Lock	1	1	Programmable	[8],[9]
					Write R32[7] = '0'					[8],[10]
					PWR_GOOD --> Low					[9],[11]
					Internal VR Disable Fault	P2_A2_Configurable_Lock	1	1	Programmable	[9],[11]
					VR_EN --> Low	P1_Configurable_Lock	1	1	N/A	[9],[12]
					Write R32[7] = '0'					[10],[12]
	1	0	0	Secure	See Table 25	DVFSQ Configurable Locked	1	0	Secure	
	1	0	0	Secure	VR_EN --> Low	P2_A1_Configurable_Lock	1	0	Secure	[8],[9]
					PWR_GOOD --> Low					[9],[11]
					Internal VR Disable Fault	P2_A2_Configurable_Lock	1	0	Secure	[9],[11]
					VR_EN --> Low	P1_Configurable_Lock	1	0	N/A	[9],[12]

**Table 26 — PMIC Security State Transition (cont'd)**

Start State					Event	End State				Notes
State	R2E[3]	Unlock Input Pin	R2F[2]	Register Status		State	R2E[3]	R2F[2]	Register Status	
P2_A1_Unlocked	0	X	1	Program mable	Write R2F[2] = '0'	P2_A1_Locked	0	0	Secure	
					Write R2E[3] = '1'	P2_A1_Unlocked	0	1	Program mable	[6]
	0	X	1	Program mable	VR_EN --> High	P3_Unlock	0	1	Program mable	[10]
					Write R32[7] = '1'					[10]
					Internal Fault (e.g., LDO fault)	P2_A2_Unlocked				[9]
P2_A2_Unlocked	0	X	1	Program mable	See Table 25	P3_Unlocked	0	1	Program mable	
	0	X	1	Program mable	Write R2F[2] = '0'	P2_A2_Locked	0	0	Secure	
					Write R2E[3] = '1'	P2_A2_Unlocked	0	1	Program mable	[6]
P2_A1_Locked	0	X	0	Secure	VR_EN --> High	P3_Locked	0	0	Secure	[10]
					Internal Fault (e.g., LDO fault)	P2_A2_Locked	0	0	Secure	
P2_A2_Locked	0	X	0	Secure	N/A	P2_A2_Locked	0	0	Secure	[13]
P2_A1_Configurable_Lock	1	1	1	Program mable	Unlock --> Low	P2_A1_Configurable_Lock	1	0	Secure	
					Write R2E[3] = '0'		1	1	Program mable	[7]
					Write R2F[2] = '0'	P2_A1_Locked	0	0	Secure	
	1	1	1	Program mable	VR_EN --> High	P3_Configurable_Lock	1	1	Program mable	
					Write R32[7] = '1'					
					Internal Fault (e.g., LDO fault)	P2_A2_Configurable_Lock				[9]
	1	0	0	Secure	Unlock --> High	P2_A1_Configurable_Lock	1	1	Program mable	
					Write R2E[3] = '0'		1	0	Secure	[7]
	1	0	0	Secure	VR_EN --> High	P3_Configurable_Lock	1	0	Secure	
					Internal Fault (e.g., LDO fault)	P2_A2_Configurable_Lock	1	0	Secure	

**Table 26 — PMIC Security State Transition (cont'd)**

Start State					Event	End State				Notes
State	R2E[3]	Unlock Input Pin	R2F[2]	Register Status		State	R2E[3]	R2F[2]	Register Status	
P2_A2_Configurable_Lock	1	1	1	Programmable	See Table 25	P3_Configurable_Lock	1	1	Programmable	
	1	1	1	Programmable	Unlock --> Low	P2_A2_Configurable_Lock	1	0	Secure	
					Write R2E[3] = '0'		1	1	Programmable	[7]
					Write R2F[2] = '0'	P2_A2_Locked	0	0	Secure	
	1	0	0	Secure	See Table 25	P3_Configurable_Lock	1	0	Secure	
	1	0	0	Secure	Unlock --> High	P2_A2_Configurable_Lock	1	1	Programmable	
					Write R2E[3] = '0'		1	0	Secure	[7]
DVFSQ_Locked	0	X	0	Secure	See Table 25	P3_Locked	0	0	Secure	
					See Table 25	P2_A2_Locked	0	0	Secure	
					See Table 25	P2_A1_Locked	0	0	Secure	
					See Table 25	P1_Locked	0	0	N/A	
	0	X	0	Secure	Write R2E[3] = '1'	DVFSQ_Locked	0	0	Secure	
DVFSQ_Unlocked	0	X	1	Programmable	See Table 25	P3_Unlocked	0	1	Programmable	
					See Table 25	P2_A2_Unlocked	0	1	Programmable	
					See Table 25	P2_A1_Unlocked	0	1	Programmable	
					See Table 25	P1_Locked	0	1	N/A	
	0	X	1	Programmable	Write R2F[2] = '0'	DVFSQ_Locked	0	0	Secure	
					Write R2E[3] = '1'	DVFSQ_Unlocked	0	1	Programmable	[6]



**Table 26 — PMIC Security State Transition (cont'd)**

Start State					Event	End State				Notes
State	R2E[3]	Unlock Input Pin	R2F[2]	Register Status		State	R2E[3]	R2F[2]	Register Status	
DVFSQ_Configurable_Lock	1	1	1	Program mable	See Table 25	P3_Configurable_Locked	1	1	Program mable	
					See Table 25	P2_A2_Configurable_Lock	1	1	Program mable	
					See Table 25	P2_A1_Configurable_Lock	1	1	Program mable	
					See Table 25	P1_Configurable_Lock	1	1	Program mable	
	1	1	1	Program mable	Unlock --> Low	DVFSQ_Configurable_Lock	1	0	Secure	
					Write R2E[3] = '0'		1	1	Program mable	[7]
					Write R2F[2] = '0'	DVFSQ_Locked	0	0	Secure	
	1	0	0	Secure	See Table 25	P3_Configurable_Locked	1	0	Secure	
					See Table 25	P2_A2_Configurable_Lock	1	0	Secure	
					See Table 25	P2_A1_Configurable_Lock	1	0	Secure	
					See Table 25	P1_Configurable_Lock	1	0	Secure	
	1	0	0	Secure	Unlock --> High	DVFSQ_Configurable_Lock	1	1	Program mable	
					Write R2E[3] = '0'		1	0	Secure	[7]

NOTE 1 The PMIC requires power cycle to enable P2\_B, P3\_Unlocked, or P3\_Configurable\_lock security states.

NOTE 2 The PMIC operates in unlocked state where all registers are in programmable mode. The host can write R2F[2] to '0' and PMIC enters in secure mode. Power cycle is required to enable P2\_B, P3\_Unlocked or P3\_Configurable\_lock states. Note: After VR\_EN command, if host writes R2E[3] = 1 to enable the Unlock input pin receiver and then writes R2F[2] = '0', the PMIC still enters secure mode but keeps the R2E[3] = '0' and keeps the Unlock input pin receiver disabled.

NOTE 3 The PMIC samples the Unlock input pin in conjunction with VR\_EN command.

NOTE 4 The PMIC updates R2F[2] register to '0' and operates in P3\_Locked state where all registers are secure (i.e., locked), updates R2E[3] register to '0' and hence disables the Unlock input pin receiver.

NOTE 5 The PMIC operates in P3\_Configurable lock states where register R2F[2] = '1'.

NOTE 6 The R2E[3] register is unique. The write '1' operation to this register is ignored and PMIC keeps the Unlock input pin receiver disabled.

NOTE 7 The R2E[3] register is unique. The write '0' operation to this register is ignored and PMIC keeps the Unlock input pin receiver enabled. The R2E[3] = '0' write operation is only allowed while PMIC is in P2\_B state.

NOTE 8 R1A[4] = '0'

NOTE 9 PWR\_GOOD output = Low

NOTE 10 PWR\_GOOD output = Float

NOTE 11 R1A[4] = X (either '0' or '1')

NOTE 12 R1A[4] = '1'

NOTE 13 Requires power cycle.

## 4.12 DVFSQ\_n Pin Function and DVFSQ State

DVFSQ (Dynamic Voltage and Frequency Scaling of the VDDQ (SWB) rail) is a low power state for LPDDR5 memory. This state introduces power saving LPDDR5 memory by lowering the operational SWB voltage value in tandem with a reduction in memory bus speed. The change in LPDDR5 memory bus speed is controlled by the controller and is transparent to PMIC functionality.

The PMIC entry and exit to DVFSQ state is enabled by the DVFSQ\_n input pin. DVFSQ\_n is an asynchronous input signal. By default at power on, the DVFSQ\_n input pin function is disabled. The host can enable the DVFSQ\_n input pin function by setting [Table 150, Register 0x2E \[4\] = '1'](#). If PMIC is selected to operate in secure mode, this register must be written when PMIC is in P2\_B programmable state at initial power on prior to issuing first VR Enable command (either via I<sup>2</sup>C/I<sup>3</sup>C bus or with a pin). When in programmable or configurable lock mode, the DVFSQ\_n pin can be disabled at any time when [Table 114, Register 0x0A \[0\] = '0'](#). There are no restrictions on the number of times DVFSQ\_n pin can be enabled or disabled. When DVFSQ\_n pin is enabled, the voltage applied to the DVFSQ\_n input pin is identified by [Table 155, Register 0x33 \[1\]](#).

When the DVFSQ\_n input pin is enabled in the PMIC and the DVFSQ\_n pin detects high to low voltage edge transition in P3 state, the PMIC enters DVFSQ state and the PMIC SWB output voltage regulator setting switches from [Table 141, Register 0x25, \[7:1\]](#) to [Table 166, Register 0x3E \[7:1\]](#) and PMIC updates [Table 114, Register 0x0A \[0\] = '1'](#). The PMIC adjusts the SWB output voltage at a ramp rate defined in [Table 150, Register 0x2E \[7:6\]](#). When DVFSQ\_n pin detects low to high voltage edge transition, the PMIC exits DVFSQ state, SWB output voltage regulator setting switches from [Table 166, Register 0x3E \[7:1\]](#) to [Table 141, Register 0x25, \[7:1\]](#) and PMIC updates [Table 114, Register 0x0A \[0\] = '0'](#). The PMIC adjusts the SWB output voltage at a ramp rate defined in [Table 150, Register 0x2E \[7:6\]](#). During the output voltage transition, the PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to crossing of the output voltage threshold setting. However, the PMIC does assert PWR\_GOOD output signal if there are abnormal issues that triggers VR Disable command as described in Table 27. The PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32 \[5\] = '1'](#).

The PMIC DVFSQ state can only be entered from the P3 state. When operating in the PMIC DVFSQ state, the PMIC exits the DVFSQ state upon VR Disable command (either via I<sup>2</sup>C/I<sup>3</sup>C bus or with VR\_EN pin), updates [Table 114, Register 0x0A \[0\] = '0'](#) and prohibits re-entry until a high to low voltage edge transition is detected by the DVFSQ\_n input pin while operating in the P3 state.

It is not permitted to change the SWB output voltage related settings ([Table 141, Register 0x25, \[7:1\]](#), [Table 147, Register 0x2B, \[3\]](#), [Table 166, Register 0x3E \[7:1\]](#), and [Table 167, Register 0x3F \[2\]](#)) when PMIC [Table 114, Register 0x0A \[0\] = '1'](#). These registers must be locked when PMIC is in DVFSQ state regardless of whether PMIC enters DVFSQ state from P3\_Unlocked or P3\_Configurable\_Lock state.

#### 4.12 DVFSQ\_n Pin Function and DVFSQ State (cont'd)

These registers are unlocked when PMIC exits DVFSQ state however they may be still locked if PMIC is operating in P3\_Locked state or P3\_Configurable\_Lock if Unlock input is low.

Note that platform power sequencing may energize the voltage powering the DVFSQ\_n input signal of the PMIC prior to turning on the VIN\_Bulk input supply voltage of the PMIC. This can potentially induce a 'back-drive' voltage from the DVFSQ\_n input signal pin to the VIN\_Bulk rail. Since this can induce system instability, the PMIC must block all 'back-drive' paths.

#### 4.13 SWB\_Disable Input Pin Function

The PMIC offers a method to override SWB output rail enable function in power on sequence config0 to power on sequence config3 registers. The SWB\_Disable input pin, if enabled, communicates to PMIC to not turn on SWB output regulator even if SWB output regulator is enabled in power on sequence config0 to config3 register.

By default, the SWB\_Disable input pin is enabled when PMIC powers up. The host can disable the SWB\_Disable pin by clearing register [Table 150, Register 0x2E](#) [5] = '0'.

When the SWB\_Disable input pin is disabled, the PMIC input receiver is off and PMIC follows the power on sequence config0 to power on sequence config3 registers and turns on appropriate rails as configured. The status register [Table 173, Register 0x109](#) [0] does not apply and it may be either '0' or '1'.

When SWB\_Disable input pin is enabled, the PMIC checks the SWB\_Disable input pin level status at the time of VR Enable command (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on).

- If the SWB\_Disable input pin is low, the PMIC updates the status register [Table 173, Register 0x109](#) [0] to '0' and executes power on sequence config 0 to power on sequence config3 registers and turns on all rails including SWB accordingly as configured.
- If the SWB\_Disable input pin is high, the PMIC updates the status register [Table 173, Register 0x109](#) [0] to '1', executes power on sequence config 0 to power on sequence config3 registers and turns on all rails except for SWB output rail. The PMIC overrides the SWB output rail in all four power on sequence config0 to config3 registers and ensures that PMIC does not turn on SWB output regulator. The PMIC follows all settings including the idle delay as configured in power on sequence config0 to power on sequence config3 registers.

#### 4.14 VR\_EN Input Pin Function

The PMIC offers a method to turn on and turn off all output rails with a VR\_EN input pin.

When valid VIN\_Bulk and VIN input supplies are present, the PMIC executes VR Enable command ([Table 154, Register 0x32](#) [7] = '1') when VR\_EN input pin is asserted to High. The PMIC executes power on sequence configuration registers ([Table 182, Register 0x40](#) to [Table 185, Register 0x43](#)) and floats PWR\_GOOD signal. The VR\_EN pin must remain at stable high level for entire power on sequence.

The PMIC executes VR Disable command ([Table 154, Register 0x32](#) [7] = '0') when VR\_EN input pin is de-asserted to Low. The PMIC executes power off sequence configuration registers ([Table 200, Register 0x58](#) to [Table 203, Register 0x5B](#)) and asserts PWR\_GOOD signal Low. The VR\_EN pin must remain at stable low level for entire power off sequence.

## 4.15 Function Interrupt - PWR\_GOOD Output Signal

This clause defines the output functionality of PWR\_GOOD (Table 154, Register 0x32 [5] = '0') pin.

When mask register bits are not set, the PMIC asserts its GSI\_n output signal and PWR\_GOOD output signal as shown in Table 27 when any event occurs. The table also highlights 11 events that cause the PMIC to generate internally VR Disable command. For remaining events that do not trigger internal VR Disable command, the PMIC continues to operate as normal.

**Table 27 — Events Interrupt Summary**

Event	Status Bit	Clear Bit	Mask Bit	Threshold Bits	Trigger VR Disable?	PWR_GOOD Output	GSI_n Output
VIN_Bulk Power Good	R08 [7]	R10 [7]	R15 [7]	R1A [7:6]	No	Low	Low
VIN_Bulk Over Voltage	R08 [0]	R10 [0]	R15[0]	R1B [7]	Yes	Low	Low
SWA Output Power Good	R08 [5]	R10 [5]	R15 [5]	R21 [0]; R22 [7:6]	No	Low	Low
SWD Output Power Good	R08 [4]	R10 [4]	R15 [4]	R23 [0]; R24 [7:6]	No	Low	Low
SWB Output Power Good	R08 [3]	R10 [3]	R15 [3]	R25 [0]; R26 [7:6]	No	Low	Low
SWC Output Power Good	R08 [2]	R10 [2]	R15 [2]	R27 [0]; R28 [7:6]	No	Low	Low
1.8 V LDO Power Good	R09 [5]	R11 [5]	R16 [5]	R1A [2]	No	Low	Low
1.0 V LDO Power Good	R33 [2]	R14 [2]	R19 [2]	R1A [0]	No	Low	Low
SWA Output Over Voltage	R0A [7]	R12 [7]	R17[7]	R22 [5:4]	Yes	Low	Low
SWD Output Over Voltage	R0A [6]	R12 [6]	R17[6]	R24 [5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A [5]	R12 [5]	R17[5]	R26 [5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A [4]	R12 [4]	R17[4]	R28 [5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B [3]	R13 [3]	R18[3]	R22 [3:2]	Yes	Low	Low
SWD Output Under Voltage	R0B [2]	R13 [2]	R18[2]	R24 [3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B [1]	R13 [1]	R18[1]	R26 [3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B [0]	R13 [0]	R18[0]	R28 [3:2]	Yes	Low	Low
VIN_Bulk Input Under Voltage	R33[3]	R14[3]	R19[3]	Vendor Specific	Yes	Low	Low
SWA Output Current Limit	R0B [7]	R13 [7]	R18 [7]	R20 [7:6]	No	High	Low
SWD Output Current Limit	R0B [6]	R13 [6]	R18 [6]	R20 [5:4]	No	High	Low
SWB Output Current Limit	R0B [5]	R13 [5]	R18 [5]	R20 [3:2]	No	High	Low
SWC Output Current Limit	R0B [4]	R13 [4]	R18 [4]	R20 [1:0]	No	High	Low
SWA Output High Current/Power	R09 [3]	R11 [3]	R16 [3]	R1C [7:2]	No	High	Low
SWD Output High Current/Power	R09 [2]	R11 [2]	R16 [2]	R1D [7:2]	No	High	Low
SWB Output High Current/Power	R09 [1]	R11 [1]	R16 [1]	R1E [7:2]	No	High	Low
SWC Output High Current/Power	R09 [0]	R11 [0]	R16 [0]	R1F [7:2]	No	High	Low
High Temperature Warning	R09 [7]	R11 [7]	R16 [7]	R1B [2:0]	No	High	Low
Critical Temperature	R08 [6]	N/A	N/A	R2E [2:0]	Yes	Low	Low
PEC Error	R0A [3]	R12 [3]	R17 [3]	N/A	No	High	Low
Parity Error	R0A [2]	R12 [2]	R17 [2]	N/A	No	High	Low
DVFSQ_n Pin	R33[1]	N/A	N/A	N/A	No	High	N/A
Unlock Pin	R33[0]	N/A	N/A	N/A	No	High	N/A
SWB_Disable Pin	R109[0]	N/A	N/A	N/A	No	High	N/A

#### 4.15 Function Interrupt - PWR\_GOOD Output Signal (cont'd)

The host is expected to read appropriate status registers to determine and isolate the cause of GSI\_n signal or PWR\_GOOD signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI\_n signal or PWR\_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. [Table 28](#) and [Table 29](#) show the PMIC's response of GSI\_n signal and PWR\_GOOD output signal for each event before and after host issues the Clear command. [Table 28](#) and [Table 29](#) assume that all mask bits are either '0' or '1' for simplicity.

**Table 28 — PMIC Response for Clear Command by Host - 1**

	Event Occurred; All Mask Bits = '0'		Clear Command; Event Not Present; All Mask Bits = '0'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
			R2F [1:0] = '00' or '01' or '10'		R2F [1:0] = '00'		R2F [1:0] = '00'	
Event	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_Bulk Power Good	Low	Low	High	High	Low	High	High	High
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWD Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
1.8 V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0 V LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_Bulk Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWD Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWD Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C <sup>[1]</sup>	P/C <sup>[1]</sup>	Low	Low	P/C <sup>[1]</sup>	P/C <sup>[1]</sup>
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

NOTE 1 P/C = Power Cycle

#### 4.15 Function Interrupt - PWR\_GOOD Output Signal (cont'd)

**Table 29 — PMIC Response for Clear Command by Host - 2**

	Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'		Event Occurred; All Mask Bits = '1'		Clear Command; Event Not Present; All Mask Bits = '1'	
	R2F [1:0] = '01'		R2F [1:0] = '01'		R2F [1:0] = '10'		R2F [1:0] = '10'	
Event	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_Bulk Power Good	High	Low	High	High	High	High	High	High
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWD Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
1.8 V LDO Power Good	High	Low	High	High	High	High	High	High
1.0 V LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWD Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
VIN_Bulk Input Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWD Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWD Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	P/C <sup>[1]</sup>	P/C <sup>[1]</sup>	Low	Low	P/C <sup>[1]</sup>	P/C <sup>[1]</sup>
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

NOTE 1 P/C = Power Cycle.

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI\_n output signal or PWR\_GOOD output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI\_n output signal and the assertion of PWR\_GOOD output signal.

#### 4.15.1 Input Power Good Status

There is one possibility where PMIC recognizes the input supply fail.

1. VIN\_Bulk goes below the threshold set in register [Table 130, Register 0x1A](#) [7:6]

When this event occurs for a period longer than tInput\_PWR\_GOOD\_GSI\_Assertion time, then PMIC sets the register [Table 112, Register 0x08](#) [7] and drives GSI\_n and PWR\_GOOD output signal as shown in [Table 27](#) at the same time.

The PMIC allows access to all registers and PMIC continues to operate as normal as long as VIN\_Bulk input remains above 3.0 V. See also Section 4.15.5. The host is responsible for taking any specific action. The host may clear the VIN\_Bulk input power good status register by writing '1' to register [Table 120, Register 0x10](#) [7] or by writing '1' to global status clear register [Table 124, Register 0x14](#) [0]. If the input power not good condition is still present, then PMIC will continue to drive GSI\_n and PWR\_GOOD output signal as in [Table 27](#) and the status register [Table 112, Register 0x08](#) [7] will remain at '1'. If the input power not good condition persists, the host may set the appropriate mask register to remove GSI\_n or PWR\_GOOD output signal as shown in [Table 28](#) and [Table 29](#).

#### 4.15.2 Input Over Voltage Protection

An input over voltage protection mechanism is implemented to limit the voltages to the PMIC. The PMIC actively monitors the input voltage VIN\_Bulk rail.

There is one possibility where PMIC recognizes the input over voltage event.

1. VIN\_Bulk input goes above the threshold set in register [Table 131, Register 0x1B](#) [7].

When this event occurs for a period longer than tInput\_OV time, then PMIC sets the register [Table 112, Register 0x08](#) [0]. Note that at this point, the PMIC does not assert PWR\_GOOD output signal. The PMIC allows access to all registers and PMIC continues to operate as normal. The host is responsible for taking any specific action. The host may clear the VIN\_Bulk input over voltage status register by writing '1' to register [Table 120, Register 0x10](#) [0] or by writing '1' to global status clear register [Table 124, Register 0x14](#) [0]. If the input over voltage condition is still present then PMIC continues to assert the status register [Table 112, Register 0x08](#) [0] to '1'.

In programmable mode (i.e., [Table 151, Register 0x2F](#) [2] = '1'), if VIN\_Bulk input supply over voltage condition persists greater than tInput\_OV\_VR\_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR\_GOOD signal. The PMIC keeps its VOUT\_1.8V and VOUT\_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR\_GOOD signal assertion. Once host determines the cause, the host must first clear the VIN\_Bulk input over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register [Table 124, Register 0x14](#) [0]. If the input over voltage condition is still present then PMIC continues to assert the status register [Table 112, Register 0x08](#) [0] to '1'. Once the status register is cleared, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR\_GOOD signal is floated when all of its output regulators are normal and input over voltage condition is no longer present.



#### 4.15.2 Input Over Voltage Protection (cont'd)

In secure mode (i.e., [Table 151, Register 0x2F](#) [2] = '0'), if VIN\_Bulk input supply over voltage condition persists greater than tInput\_OV\_VR\_Disable time then PMIC internally generates VR Disable command and disables all of its switching output regulators and asserts PWR\_GOOD signal. The PMIC keeps its VOUT\_1.8V and VOUT\_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

#### 4.15.3 Output Power Good Status

The PMIC provides the voltage tolerance information to host that its output regulator may have crossed the desired DC+AC voltage tolerance from its nominal programmed setting. The nominal programmed setting for output regulator SWA, SWD, SWB, and SWC is programmed in register [Table 137, Register 0x21](#), [7:1], [Table 139, Register 0x23](#), [7:1], [Table 141, Register 0x25](#), [7:1], and [Table 143, Register 0x27](#), [7:1], respectively. The PMIC offers the PWR\_GOOD condition to be set independently for low side and high side.

In addition, PMIC has two LDO regulators: VOUT\_1.8V and VOUT\_1.0V

There are four possibilities where PMIC recognizes the output power good event for any output regulator.

1. Output voltage goes below the threshold set in register [Table 137, Register 0x21](#), [0] for SWA, or [Table 139, Register 0x23](#), [0] for SWD, or [Table 141, Register 0x25](#), [0] for SWB, or [Table 143, Register 0x27](#), [0] for SWC.
2. Output voltage goes above the threshold set in register [Table 138, Register 0x22](#), [7:6] for SWA, or [Table 140, Register 0x24](#) [7:6] for SWD, or [Table 142, Register 0x26](#), [7:6] for SWB, or [Table 144, Register 0x28](#), [7:6] for SWC.
3. LDO output VOUT\_1.8V goes below the threshold set in register [Table 130, Register 0x1A](#) [2].
4. LDO output VOUT\_1.0V goes below the threshold set in register [Table 130, Register 0x1A](#) [0].

When either event occurs for a period longer than tOutput\_PWR\_GOOD\_Assertion time, then PMIC sets the register [Table 112, Register 0x08](#) [5:2] or [Table 113, Register 0x09](#) [5] or [Table 155, Register 0x33](#) [2] appropriately and asserts PWR\_GOOD signal as shown in [Table 27](#) at the same time. The PMIC may continue to operate but PMIC5200 functionality may not be guaranteed. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine and identify the cause of the PWR\_GOOD signal assertion. Once host determines the cause, the host may clear the appropriate status register individually or by writing '1' to global status clear register [Table 124, Register 0x14](#) [0] and PMIC floats the PWR\_GOOD signal. If the output power not good condition is still present then PMIC continues to assert PWR\_GOOD signal and the appropriate status register [Table 112, Register 0x08](#) [5:2], or [Table 113, Register 0x09](#) [5], or [Table 155, Register 0x33](#) [2] remains at '1'.



#### 4.15.4 Output Over Voltage Protection

An output over voltage protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulator.

There are four possibilities where PMIC recognizes the over voltage event.

1. SWA output regulator goes above the threshold set in register [Table 138, Register 0x22](#), [5:4].
2. SWD output regulator goes above the threshold set in register [Table 140, Register 0x24](#), [5:4].
3. SWB output regulator goes above the threshold set in register [Table 142, Register 0x26](#), [5:4].
4. SWC output regulator goes above the threshold set in register [Table 144, Register 0x28](#), [5:4].

In programmable mode (i.e., [Table 151, Register 0x2F](#) [2] = '1'), if any output over voltage condition persists greater than tOutput\_OV\_VR\_Disable time, then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register [Table 114, Register 0x0A](#) [7:4] appropriately, and asserts PWR\_GOOD output signal. The PMIC keeps its VOUT\_1.8V and VOUT\_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR\_GOOD signal assertion. Once host determines the cause, the host must first clear the appropriate output over voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register [Table 124, Register 0x14](#) [0]. Once the status register is cleared, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command. The PMIC enables output switching regulators and ensures PWR\_GOOD signal is floated when all of its output regulators are normal.

In secure mode (i.e., [Table 151, Register 0x2F](#) [2] = '0'), if any output over voltage condition persists greater than tOutput\_OV\_VR\_Disable time, then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register [Table 114, Register 0x0A](#) [7:4] appropriately, and asserts PWR\_GOOD. The PMIC keeps its VOUT\_1.8V and VOUT\_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

#### 4.15.5 Output Under Voltage and VIN\_Bulk Under Voltage Lockout Protection

An output under voltage lockout protection mechanism is implemented to limit the voltages on the PMIC output regulators. The PMIC actively monitors the output voltage on each enabled regulator.

There are five possibilities where PMIC recognizes the under voltage lockout event.

1. SWA output regulator goes below the threshold set in register [Table 138, Register 0x22](#), [3:2].
2. SWD output regulator goes below the threshold set in register [Table 140, Register 0x24](#) [3:2].
3. SWB output regulator goes below the threshold set in register [Table 142, Register 0x26](#), [3:2].
4. SWC output regulator goes below the threshold set in register [Table 144, Register 0x28](#), [3:2].
5. VIN\_Bulk input voltage goes below vendor specific voltage.

In programmable mode (i.e., [Table 151, Register 0x2F](#) [2] = '1'), if any output under voltage condition or VIN\_Bulk input voltage condition as listed above persists greater than tOutput\_UV\_VR\_Disable time, then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register [Table 115, Register 0x0B](#) [3:0], [Table 155, Register 0x33](#) [3] appropriately, and asserts PWR\_GOOD. The PMIC keeps its VOUT\_1.8V and VOUT\_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause of the PWR\_GOOD signal assertion. Once host determines the cause, the host must first clear the appropriate output under voltage status register as well as any other relevant status registers individually or by writing '1' to global status clear register [Table 124, Register 0x14](#) [0]. Once the status register is cleared, the host may re-enable the PMIC's output switching regulator by issuing VR Enable command, assuming a valid VIN\_Bulk input voltage. The PMIC enables output switching regulators and floats PWR\_GOOD signal High when all of its output regulators are normal.

In secure mode (i.e., [Table 151, Register 0x2F](#) [2] = '0'), if any output under voltage condition or VIN\_Bulk input voltage condition as listed above persists greater than tOutput\_UV\_VR\_Disable time, then PMIC internally generates VR Disable command and disables all of its switching output regulators, sets register [Table 115, Register 0x0B](#) [3:0], [Table 155, Register 0x33](#) [3] appropriately, and asserts PWR\_GOOD. The PMIC keeps its VOUT\_1.8V and VOUT\_1.0V LDO output regulators active. The PMIC allows access to all registers. The host is responsible for taking the action of power cycling the PMIC.

#### 4.15.6 Output Current Limiter Warning Event

The PMIC has output current limiter mechanism to limit the current on the PMIC output voltage regulators. This feature is supported regardless of whether ADC is enabled or disabled.

There are four possibilities where PMIC recognizes the current limiter event.

1. SWA output regulator current goes above the threshold set in register [Table 136, Register 0x20](#) [7:6].
2. SWD output regulator current goes above the threshold set in register [Table 136, Register 0x20](#) [5:4].
3. SWB output regulator current goes above the threshold set in register [Table 136, Register 0x20](#) [3:2].
4. SWC output regulator current goes above the threshold set in register [Table 136, Register 0x20](#) [1:0].

#### 4.15.6 Output Current Limiter Warning Event (cont'd)

When either event occurs for a period longer than tOutput\_Current\_Limiter time, then PMIC sets the register [Table 115, Register 0x0B \[7:4\]](#) appropriately. The PMIC continues to operate as normal and PWR\_GOOD output remains high as shown [Table 27](#). The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space. Once host determine the cause, the host may clear the appropriate output current limiter status register as well as any other status registers individually or by writing '1' to global status clear register in [Table 124, Register 0x14 \[0\]](#). If the output current limiter condition is still present then PMIC continues to assert the appropriate status register in [Table 115, Register 0x0B \[7:4\]](#) to '1'.

#### 4.15.7 Output High Current Consumption Warning Event

The PMIC supports high output current consumption warning mechanism for each of its regulator output. If ADC is enabled ([Table 152, Register 0x30 \[7\] = '1'](#)), the PMIC actively monitors the average output current of the regulator and reports high output current consumption warning.

There are four possibilities where PMIC recognizes the high output current consumption.

1. SWA output regulator average current goes above the threshold set in register [Table 132, Register 0x1C \[7:0\]](#).
2. SWD output regulator average current goes above the threshold set in register [Table 133, Register 0x1D \[7:0\]](#).
3. SWB output regulator average current goes above the threshold set in register [Table 134, Register 0x1E \[7:0\]](#).
4. SWC output regulator average current goes above the threshold set in register [Table 135, Register 0x1F \[7:0\]](#).

When either event occurs then PMIC sets the register [Table 113, Register 0x09 \[3:0\]](#) appropriately. The PMIC continues to operate as normal and PWR\_GOOD output remains high as shown [Table 27](#). The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space. Once host determines the cause, the host may clear the appropriate output current consumption warning status register as well as any other status registers individually or by writing '1' to global status clear register in [Table 124, Register 0x14 \[0\]](#). If the output current consumption warning condition is still present then PMIC continues to assert the appropriate status register in [Table 113, Register 0x09 \[3:0\]](#) to '1'.

#### 4.15.8 PMIC High Temperature Warning and Critical Temperature Protection

The PMIC provides a high temperature warning mechanism, as well as a critical temperature shutdown. This feature is supported regardless of whether ADC is enabled or disabled. There are two registers associated with PMIC temperature: The high temperature warning threshold register [Table 131, Register 0x1B \[2:0\]](#) and shutdown temperature threshold register [Table 150, Register 0x2E \[2:0\]](#). The value programmed in the shutdown temperature register must be equal or greater than value programmed in a warning threshold register.

There is one possibility where PMIC recognizes the high temperature event.

1. The PMIC temperature goes above the threshold set in register [Table 131, Register 0x1B \[2:0\]](#).

#### 4.15.8 PMIC High Temperature Warning and Critical Temperature Protection (cont'd)

When the high-temperature event occurs for a period longer than tHigh\_Temp\_Warning time, the PMIC sets the register [Table 113, Register 0x09](#) [7]. The PMIC continues to operate as normal. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause. Once host determines the cause, the host may clear the temperature warning status register, as well as any other status registers individually or by writing '1' to global status clear register in [Table 124, Register 0x14](#) [0]. If the high temperature warning condition is still present, then PMIC continues to status register in [Table 113, Register 0x09](#) [7] to '1'.

If the PMIC temperature goes above the threshold set in register [Table 150, Register 0x2E](#) [2:0] for a period longer than tShut\_Down\_Temp time, the PMIC internally generates VR Disable command and disables all of its switching output regulators, sets the code in register [Table 109, Register 0x05](#) [2:0], updates [Table 112, Register 0x08](#) [6], and PWR\_GOOD output signal as shown in [Table 27](#) at the same time. The PMIC keeps its VOUT\_1.8V LDO and VOUT\_1.0V LDO output regulator active. The PMIC allows access to all registers. The host is responsible for taking any specific action. The host is expected to monitor the temperature status registers. When the temperature drops below the threshold, the host must re-start the PMIC by going through the power cycle of the VIN\_Bulk input supply.

#### 4.15.9 Packet Error Code (PEC) and Parity Error Event

In I3C mode, PEC function and parity function can be enabled. If enabled, when PMIC detects either PEC error or parity error, the PMIC sets the register [Table 114, Register 0x0A](#) [3:2] appropriately, and it continues to operate as normal and allows access to all registers. See clause 5.4.5 to 5.4.9 for additional details. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in [Table 124, Register 0x14](#) [0].

In I<sup>2</sup>C mode, for supported CCC, the PMIC supports parity function. When PMIC detects parity error, the PMIC sets the register [Table 114, Register 0x0A](#) [2], and it continues to operate as normal and allows access to all registers. See Section 5.4.6 to 5.4.9 for additional details. The host is responsible for taking any specific action. The host may query the PMIC register space to determine the cause. Once host determines the cause, the host may clear the status register individually or by writing '1' to global status clear register in [Table 124, Register 0x14](#) [0].

#### 4.16 Analog to Digital Converter (ADC)

The PMIC supports analog to digital converter (ADC) to monitor input supply voltages (VIN\_Bulk), as well as output voltage regulator voltage (SWA, SWD, SWB, SWC, VOUT\_1.8V, and VOUT\_1.0V). The register [Table 152, Register 0x30](#) [7:3] allows to enable the ADC and select the input supply voltage or desired output supply voltage. The register [Table 153, Register 0x31](#) [7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is shown in [Table 30](#) and [Table 31](#).

**Table 30 — PMIC Output Voltage ADC Accuracy**

Output Regulator; Voltage Range	SWA	SWD	SWB	SWC	1.8V LDO 1.0V LDO	VBIAS
1050 mV to 1160 mV	± 1 LSB	N/A	N/A	N/A	N/A	N/A
Less than 1050 mV; greater than 1160 mV	± 3 LSB	N/A	N/A	N/A	N/A	N/A

**Table 30 — PMIC Output Voltage ADC Accuracy (cont'd)**

Output Regulator; Voltage Range	SWA	SWD	SWB	SWC	1.8V LDO 1.0V LDO	VBIAS
850 mV to 950 mV	N/A	$\pm 1$ LSB	N/A	N/A	N/A	N/A
Less than 850 mV; greater than 950 mV	N/A	$\pm 3$ LSB	N/A	N/A	N/A	N/A
450 mV to 550 mV	N/A	N/A	$\pm 3$ LSB	N/A	N/A	N/A
Less than 450 mV; greater than 550 mV	N/A	N/A	$\pm 5$ LSB	N/A	N/A	N/A
1750 mV to 1850 mV	N/A	N/A	N/A	$\pm 1$ LSB	N/A	N/A
Less than 1750 mV; greater than 1850 mV	N/A	N/A	N/A	$\pm 3$ LSB	N/A	N/A
1.8V LDO, 1.0V LDO	N/A	N/A	N/A	N/A	$\pm 3$ LSB	N/A
VBIAS	N/A	N/A	N/A	N/A	N/A	$\pm 6$ LSB

**Table 31 — PMIC Input Voltage ADC Accuracy**

Input Voltage	
VIN_Bulk	$\pm 6$ LSB

The PMIC also monitors output voltage regulator current or power for SWA, SWD, SWB and SWC. The PMIC updates registers [Table 116, Register 0x0C \[7:0\]](#) to [Table 119, Register 0x0F \[7:0\]](#) for SWA to SWD respectively if [Table 154, Register 0x32 \[1:0\] = '00'](#) or [Table 168, Register 0x100 \[7:0\]](#) to [Table 172, Register 0x105 \[7:0\]](#) for SWA to SWD respectively if [Table 154, Register 0x32 \[1:0\] = '01'](#).

The register [Table 131, Register 0x1B \[6\]](#) allows host to select whether PMIC should report current measurements or power measurements. The current or power measurement reported in these registers are an average measurement over vendor specific time period. If [Table 131, Register 0x1B \[6\] = '1'](#), the register [Table 130, Register 0x1A \[1\]](#) allows host to select whether PMIC should report individual rail power or total power in [Table 116, Register 0x0C \[7:0\]](#) if [Table 154, Register 0x32 \[1:0\] = '00'](#) or in [Table 169, Register 0x102 \[7:0\]](#) if [Table 154, Register 0x32 \[1:0\] = '01'](#).

The register update frequency of this register is configured in [Table 152, Register 0x30 \[1:0\]](#). The internal sampling rate of the PMIC is vendor specific.

**Table 32 — PMIC ADC Current and Power Accuracy; R32[1:0] = 00**

Load Current	SWA to SWD Rails - Current Accuracy	SWA to SWD Rails - Corresponding Power Accuracy	Total Power Accuracy
Less than 0.5 A	$\pm 4$ LSB	$\pm 7$ LSB	$\pm 12$ LSB
Greater than or equal to 0.5 A	$\pm 3$ LSB	$\pm 6$ LSB	

## 4.16 Analog to Digital Converter (ADC) (cont'd)

**Table 33 — PMIC ADC Current and Power Accuracy; R32[1:0] = 01**

Load Current	SWA to SWD Rails - Current Accuracy	SWA to SWD Rails - Corresponding Power Accuracy	Total Power Accuracy
Less than 0.5 A	$\pm 9$ LSB	$\pm 15$ LSB	$\pm 25$ LSB
Greater than or equal to 0.5 A	$\pm 8$ LSB	$\pm 12$ LSB	

## 4.17 PMIC Address ID (PID)

The PMIC5200 has PID input pin which allows to assign up to three different unique ID for I<sup>2</sup>C and I<sup>3</sup>C Basic protocol.

At first power on, when VIN\_Bulk input is applied, the PMIC automatically determines its ID. The PMIC offers three different ID as shown in [Table 34](#).

**Table 34 — PMIC ID**

PID Pin Connection on CAMM2 Board	PMIC ID	Comment
short to GND	PID = 1001	
Floating	PID = 1000	
short to 1.8	PID = 1100	Connected to PMIC's VOUT_1.8V Rail

## 4.18 Error Injection

The PMIC5200 offers error injection function for the purpose of debug, test, and validation at various stages.

### 4.18.1 Error Injection - Prior to VR Enable (either via VR\_EN Pin or I<sup>2</sup>C/I<sup>3</sup>C Bus)

Prior to VR Enable command, the Error injection function may be invoked by setting error injection enable bit [Table 157, Register 0x35 \[7\] = '1'](#) during the configuration state. If any of either VIN\_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected prior to VR Enable command, the PMIC shall not execute power on sequence and shall not enable PMIC output regulators when PMIC receives VR Enable command. The PMIC shall not update error log registers ([Table 108, Register 0x04](#) to [Table 110, Register 0x06](#)). The PMIC shall update appropriate status registers ([Table 112, Register 0x08](#) to [Table 115, Register 0x0B](#), [Table 155, Register 0x33](#)) accordingly. The PMIC shall enter in secure mode if [Table 151, Register 0x2F \[2\] = '0'](#) and programmable mode if [Table 151, Register 0x2F \[2\] = '1'](#).

#### 4.18.2 Error Injection - After VR Enable (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C Bus)

After PMIC output regulators are enabled with VR Enable command and if PMIC is in programmable mode, the error injection function may be invoked by setting error injection enable bit [Table 157, Register 0x35 \[7\]](#) = '1'.

If any of either VIN\_Bulk UV/OV or SWx OV/UV or Critical Temp Shutdown error is injected the PMIC shall execute Power Off Sequence to disable PMIC output regulators and shall update the error log registers ([Table 108, Register 0x04](#) to [Table 110, Register 0x06](#)) as well as status registers ([Table 112, Register 0x08](#) to [Table 115, Register 0x0B](#), [Table 155, Register 0x33](#)) accordingly. Note that if any of the output rails are not enabled through power on sequence configuration registers, the error injection on those output rails do not apply.

After PMIC output regulators are enabled with VR Enable command and if PMIC is in secure mode, the error injection enabling [Table 157, Register 0x35 \[7\]](#) = '1' is disallowed. The PMIC shall ignore any attempts to inject any error and shall not execute Power Off Sequence to disable PMIC output regulators and shall not update any error log or status registers.

To exit the error injection function, the host shall power cycle VIN\_Bulk input supply.

#### 4.19 Acoustic Noise

The CAMM2 PMIC buck regulators normally operates in DCM (Discontinuous Current Mode). The buck regulator's switching frequency is a function of a current load on its output regulator. At light load (typically < 50 mA), the buck regulator's switching frequency may approach to less than 100 KHz.

The human ear audible frequency range is 20 Hz to 20 KHz. If buck regulator switching frequency falls within the human ear audible frequency range, then the human ear can experience the acoustic noise.

To prevent the acoustic noise to human ear, the PMIC offers a feature which prevents the buck regulator switching frequency to go below the threshold frequency that is configured in register [Table 158, Register 0x36 \[3:1\]](#). When the feature is enabled, the PMIC ensures that its switching frequency stays above the threshold frequency regardless of how low the output load current may be.

The acoustic noise prevention control feature is in [Table 158, Register 0x36 \[3:1\]](#). The control register applies to all four buck regulators. This feature is not applicable to any buck regulator that is configured to operate as Forced CCM (Continuous Current Mode). If PMIC is configured such that one or more buck regulators is configured as DCM and other buck regulator is configured as Forced CCM, when this feature is enabled, it applies to any buck regulators that are configured as DCM.

At light load, when this feature is enabled, there may be a slight difference in efficiency. However, the difference in efficiency may be insignificant and may be within the measurement noise.



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## 5 I<sup>2</sup>C and I<sup>3</sup>C Basic Operation

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At power on, by default, the PMIC device comes up in I<sup>2</sup>C mode of operation. Following applies in I<sup>2</sup>C mode:

1. The max operation speed is limited to 1 MHz
1. In-band interrupts are not supported
1. Bus reset is supported.
1. Parity check is not supported except for supported CCCs.
1. Packet Error check is not supported.

The PMIC device shall operate in the I<sup>2</sup>C mode until put into I<sup>3</sup>C Basic mode via command.

The host may put the PMIC device in I<sup>3</sup>C Basic mode by issuing SETAASA CCC.

Following applies in I<sup>3</sup>C Basic mode.

1. The max operation speed is up to 12.5 MHz
2. In-band interrupts are supported
3. Bus reset is supported.
4. Parity check is always enabled by default.
5. Packet error check is supported and by default is disabled.

### 5.1 Device Interface - Protocol

#### 5.1.1 Management Bus

The PMIC supports two different protocol on its management bus.

- I<sup>2</sup>C Target Protocol - Speed Up to 1 MHz
- I<sup>3</sup>C Basic Target Protocol - Speed Up to 12.5 MHz

The PMIC's 7-bit target address [7:1] is composed of 4-bit device address [7:4] and 3-bit HID address [3:1].

The PMIC's 4-bit device address [7:4] is:

- If PID pin is tied to GND on PCB: '1001'
- If PID pin is tied to 1.8 V on PCB: '1100'
- If PID pin floating on PCB: '1000'

The PMIC's 3-bit HID address [3:1] is per [Table 156, Register 0x34](#) [3:1].

#### 5.1.2 Switch from I<sup>2</sup>C mode to I<sup>3</sup>C Basic Mode

By default, when PMIC first powers on, it operates in I<sup>2</sup>C mode. The PMIC shall operate in I<sup>2</sup>C mode until put into I<sup>3</sup>C Basic mode via command.

In I<sup>2</sup>C mode, the host is allowed to issue only 3 CCCs (DEVCTRL, SETHID, and SETAASA). All other CCC are not supported and the PMIC device simply ignores it. The host must issue DEVCTRL or SETHID CCC first (if required) followed by SETAASA CCC.



### 5.1.2 Switch from I<sup>2</sup>C mode to I3C Basic Mode (cont'd)

The host puts the PMIC in I3C Basic mode by issuing SETAASA CCC. See also Section 5.4.10.4. When SETHID CCC is registered by the PMIC, it updates Table 156, Register 0x34 [3:1]. When SETAASA CCC is registered by the PMIC, it updates Table 154, Register 0x32 [6] to '1'.

### 5.1.3 Switch from I3C Basic Mode to I<sup>2</sup>C mode

The host can put the PMIC back in I<sup>2</sup>C mode from I3C Basic mode at any time by issuing RSTDAA CCC. When RSTDAA CCC is registered by the PMIC, it updates Table 154, Register 0x32 [6] to '0'. See also Clause 5.4.10.3.

## 5.2 Configuration Register Addressing

At first power on, by default, the PMIC accepts one byte address which covers first 256 bytes of configuration registers. To address configuration registers beyond first 256 bytes (up to 4096 bytes), the PMIC must be in a two byte address mode. The two byte address mode is configured by setting Table 152, Register 0x30 [2] = '1'. The PMIC supports one byte and two byte address mode in both I2C and I3C mode of operation.

The PMIC returns to one byte address mode when Bus Reset event occurs or when it registers RSTDAA CCC.

## 5.3 I<sup>2</sup>C Target Protocol

The PMIC device operates on a standard I<sup>2</sup>C serial interface. Transactions where the PMIC device is the targeted target device begin with the Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK.

The PMIC device host region registers that are write protected in secure mode of operation, the PMIC ACKs the host request but the PMIC does not execute the operation internally.

Similarly, regardless of secure mode or programmable mode of operation, without the correct password, all CAMM2 vendor region and vendor specific region registers are write protected and PMIC ACKs the host request but the PMIC does not execute the operation internally.

### 5.3.1 Write Operation Data Packet

The PMIC supports Byte Write or Block Write operation as shown in Table 35 and Table 36 for one byte and two address mode, respectively. For Byte Write operation, only one data byte is transferred followed by Stop operation.

**Table 35 — Write Command Data Packet; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr <sup>[1]</sup>	1	X	0	X	HID			W=0	A	
	Address [7:0]								A	
	Data								A	
	Data								A	
	...								A	
	Data								A	Sr or P

NOTE 1 In I<sup>2</sup>C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I<sup>2</sup>C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

### 5.3.1 Write Operation Data Packet (cont'd)

**Table 36 — Write Command Data Packet; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr <sup>[1]</sup>	1	X	0	X	HID			W=0	A	
	Address [7:0]								A	
	0	0	0	0	Address [11:8]			A		
	Data								A	
	Data								A	
	...								A	
	Data								A	

NOTE 1 In I<sup>2</sup>C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I<sup>2</sup>C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

### 5.3.2 Read Operation Data Packet

The PMIC supports Byte Read or Block Read operation as shown in [Table 37](#) and [Table 38](#) for one byte and two address mode, respectively. For Byte Read operation, only one data byte is transferred followed by Stop operation.

**Table 37 — Read Command Data Packet; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr <sup>[1]</sup>	1	X	0	X	HID			W=0	A	
	Address [7:0]								A	
Sr	1	X	0	X	HID			R=1	A <sup>[2]</sup>	
	Data								A	
	Data								A	
	...								A	
	Data								N <sup>[3]</sup>	Sr or P

NOTE 1 In I<sup>2</sup>C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I<sup>2</sup>C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

NOTE 2 If the PMIC NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The PMIC may eventually ACK.

NOTE 3 When PMIC device reaches last byte within the region (either Host region or CAMM2 vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

### 5.3.2 Read Operation Data Packet (cont'd)

### Table 38 — Read Command Data Packet: 2 Byte Address Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr <sup>[1]</sup>	1	X	0	X	HID			W=0	A	
	Address [7:0]								A	
	0	0	0	0	Address [11:8]			A		
Sr	1	X	0	X	HID			R=1	A <sup>[2]</sup>	
	Data								A	
	Data								A	
	...								A	
	Data								N <sup>[3]</sup>	

NOTE 1 In I<sup>2</sup>C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I<sup>2</sup>C mode. Any other operation including another Repeat Start is considered an illegal operation; the PMIC may ignore it and still ACK or it may NACK.

NOTE 2 If the PMIC NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The PMIC may eventually ACK.

NOTE 3 When PMIC device reaches last byte within the region (either Host region or CAMM2 vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

### 5.3.3 Default Read Address Pointer Mode

During normal operation of the CAMM2, the host periodically polls critical information from the PMIC. The host may poll all the status registers or current or power measurement registers or the temperature register or any combination of these different types of registers. To help improve the efficiency of the I2C bus protocol, the PMIC offers a default read pointer address mode so that whenever PMIC sees the STOP operation on SCL and SDA bus, its read address pointer is always set to default address. The default read pointer address mode is enabled through register [Table 162, Register 0x3A](#) [6] and default starting address for read operation is selectable through register [Table 162, Register 0x3A](#) [5:4]. This allows host to reduce the read command data packet as shown in [Table 39](#) from [Table 37](#). The default read address pointer reduces the packet overhead by 2 bytes. The host typically enables this mode at last after VR Enable command when the normal operation begins of the CAMM2.

### Table 39 — Read Command Data Packet with Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	1	X	0	X	HID			R=1	A	
	Data								A	
	Data								A	
	...								A	
	Data								N <sup>[1]</sup>	

NOTE 1 When PMIC device reaches last byte within the region (either Host region or CAMM2 vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 vendor region or Vendor specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only Host can perform STOP operation.

## 5.4 I3C Basic Target Protocol

### 5.4.1 Write Operation Data Packet

The PMIC device operates on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit MSB first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See [Table 40](#). The “T” bit carries Parity information from the host for each byte.

The PMIC device host region registers that are write protected in secure mode of operation, the PMIC does not execute the operation internally.

Similarly, regardless of secure mode or programmable mode of operation, without the correct password, all CAMM2 vendor region and vendor specific region registers are write protected and PMIC does not execute the operation internally.

The Packet Error Code (PEC) function is disabled by default when the PMIC device is put in I3C Basic mode. The host may optionally enable this function through [Table 156, Register 0x34 \[7\]](#) or DEVCTRL CCC. If enabled, the PEC is appended at the end of all transactions. If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Write operation.

**Table 40 — Write Command Data Packet; PEC Disabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A <sup>[1],[2],[3]</sup>	Sr <sup>[4]</sup> or P
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

**Table 41 — Write Command Data Packet; PEC Disabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A <sup>[1],[2],[3]</sup>	Sr <sup>[4]</sup> or P
	Address [7:0]								T	
	0	0	0	0	Address [11:8]			T		
	Data								T	
	...								T	
	Data								T	

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

### 5.4.1 Write Operation Data Packet (cont'd)

**Table 42 — Write Command Data Packet; PEC Enabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A <sup>[1],[2],[3]</sup>	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr <sup>[4]</sup> or P

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

**Table 43 — Write Command Data Packet; PEC Enabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1],[2],[3]	
	Address [7:0]								T	
	CMD			W=0	Address [11:8]			T		
	Data								T	
	...								T	
	Data								T	
	PEC								T	

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If PMIC device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If PMIC device has no pending IBI, there is no action taken by PMIC. Table 44 and Table 46 show the I3C Basic bus write command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 46, PEC calculation does not include IBI header byte (7'h7E followed by W=0).

### 5.4.1 Write Operation Data Packet (cont'd)

**Table 44 — Write Command Data Packet with IBI Header; PEC Disabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	Sr <sup>[5]</sup> or P
	Data								T	
	...								T	
	Data								T	

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 33 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

**Table 45 — Write Command Data Packet with IBI Header; PEC Disabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	
	0	0	0	0	Address [11:8]			T		
	Data								T	
	...								T	
	Data								T	Sr <sup>[5]</sup> or P

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 33 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

### 5.4.1 Write Operation Data Packet (cont'd)

**Table 46 — Write Command Data Packet with IBI Header; PEC Enabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr <sup>[5]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

**Table 47 — Write Command Data Packet with IBI Header; PEC Enabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	
	CMD			W=0	Address [11:8]			T		
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr <sup>[5]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.

## 5.4.2 Read Operation Data Packet

The PMIC device operates on a standard I3C Basic serial interface. Transactions where the PMIC device is the targeted target device begin with the I3C Basic Host issuing a START condition followed by a 7-bit PMIC device address then a read or write bit, RW. All data are transmitted with the most significant bit (MSB) first. During the address followed by R/W bit transmission, the PMIC device typically replies with an ACK unless there are exceptional conditions when it may passively assert a NACK. See [Table 48](#). The “T” bit carries Parity information from the host for each byte prior to Repeat START. After Repeat START, “T” bit carries information from PMIC device to Host indicating Continuous (‘1’) or Stop (‘0’) whether it is transmitting the last byte or not.

The Packet Error Code (PEC) function is disabled by default when PMIC device is put in I3C Basic mode. The host may optionally enable this function through [Table 156, Register 0x34 \[7\]](#) or DEVCTRL CCC. If enabled, the PEC is appended as shown in [Table 50](#). If PEC is enabled, the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length prematurely for Read operation.

**Table 48 — Read Command Data Packet; PEC Disabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1].[2].[3]	
	Address [7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N[4].[5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6].[7]	Sr[8] or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 34](#) to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.



## 5.4.2 Read Operation Data Packet (cont'd)

**Table 49 — Read Command Data Packet; PEC Disabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1],[2],[3]	
	Address [7:0]								T	
	0	0	0	0	Address [11:8]				T	
Sr	1	X	0	X	HID			R=1	A/N[4],[5]	
	Data								T=1	
	...								T=1	
	Data								T=1[6],[7]	Sr[8] or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 34](#) to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

## 5.4.2 Read Operation Data Packet (cont'd)

**Table 50 — Read Command Data Packet; PEC Enabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1],[2],[3]	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N <sup>[4],[5]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 <sup>[6]</sup>	Sr <sup>[7]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 35](#) to see how Host ends target device operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

## 5.4.2 Read Operation Data Packet (cont'd)

**Table 51 — Read Command Data Packet; PEC Enabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1].[2].[3]	
	Address [7:0]								T	
	CMD			R=1	Address [11:8]				T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N[4].[5]	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0[6]	Sr[7] or P

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See Figure 33 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See Figure 35 to see how Host ends target device operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

The host may optionally allow PMIC device to request IBI. For this case, the transactions to the PMIC device begin with the I3C Basic host issuing a START condition followed by 7'h7E and then write bit. If PMIC device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If PMIC device has no pending IBI, there is no action taken by PMIC. Table 52 and Table 54 show the I3C Basic bus read command data packet with optional IBI header for PEC disabled and PEC enabled case respectively. Note that in Table 54, PEC calculation (from Host to PMIC) does not include IBI header byte (7'h7E followed by W=0).

## 5.4.2 Read Operation Data Packet (cont'd)

**Table 52 — Read Command Data Packet with IBI Header; PEC Disabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N <sup>[5],[6]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1 <sup>[7],[8]</sup>	

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 7 See [Figure 34](#) to see how Host ends target device operation.

NOTE 8 When PMIC device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 9 Repeat Start or Repeat Start with 7'h7E.

## 5.4.2 Read Operation Data Packet (cont'd)

**Table 53 — Read Command Data Packet with IBI Header; PEC Disabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1].[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2.[3].[4]</sup>	
	Address [7:0]								T	
	0	0	0	0	Address [11:8]			T		
Sr	1	X	0	X	HID			R=1	A/N <sup>[5].[6]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1 <sup>[7].[8]</sup>	
										Sr <sup>[9]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 4 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 7 See [Figure 34](#) to see how Host ends target device operation.

NOTE 8 When PMIC device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 9 Repeat Start or Repeat Start with 7'h7E.

## 5.4.2 Read Operation Data Packet (cont'd)

**Table 54 — Read Command Data Packet with IBI Header; PEC Enabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N <sup>[5],[6]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 <sup>[7]</sup>	
										Sr <sup>[8]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 7 See [Figure 35](#) to see how Host ends target device operation followed by Host STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

## 5.4.2 Read Operation Data Packet (cont'd)

**Table 55 — Read Command Data Packet with IBI Header; PEC Enabled; 2 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1],[2]</sup>	
Sr	1	X	0	X	HID			W=0	A <sup>2,[3],[4]</sup>	
	Address [7:0]								T	
	CMD			R=1	Address [11:8]			T		
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N <sup>[5],[6]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 <sup>[7]</sup>	
										Sr <sup>[8]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK) and [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 7 See [Figure 35](#) to see how Host ends target device operation followed by Host STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

## 5.4.3 Default Read Address Pointer Mode

This mode works the same exact way as explained in clause 5.3.3. [Table 56](#) and [Table 57](#) show the read command data packet for PEC function disabled and enabled, respectively. When PEC function is enabled, [Table 162, Register 0x3A \[3:2\]](#) sets the number of bytes that PMIC sends out, followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in [Table 162, Register 0x3A \[3:2\]](#) register. In other words, the host must not interrupt the burst length prematurely for Default Address Pointer Read operation.

### 5.4.3 Default Read Address Pointer Mode (cont'd)

**Table 56 — Read Command Data Packet with Address Pointer Mode; PEC Disabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			R=1	A/N <sup>[1]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1 <sup>[2].[3]</sup>	

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 See Figure 34 to see how Host ends target device operation.

NOTE 3 When device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

**Table 57 — Read Command Data Packet with Address Pointer Mode; PEC Enabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			R=1	A/N <sup>[1]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 <sup>[2]</sup>	

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 See Figure 35 to see how Host ends target device operation followed by Host STOP operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

**Table 58 — Read CMD Data Packet with Address Pointer Mode and IBI Header; PEC Disabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1].2</sup>	
Sr	1	X	0	X	HID			R=1	A/N <sup>[2].[3]</sup>	
	Data								T=1	Sr <sup>[6]</sup> or P
	...								T=1	
	Data								T=1 <sup>[4].[5]</sup>	

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 33 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 4 See Figure 34 to see how Host ends target device operation.

NOTE 5 When device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 6 Repeat Start or Repeat Start with 7'h7E.



### 5.4.3 Default Read Address Pointer Mode (cont'd)

**Table 59 — Read Command Data Packet with Address Pointer Mode and IBI Header; PEC Enabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1,2]</sup>	
Sr	1	X	0	X	HID			R=1	A/N <sup>[2],[3]</sup>	
	Data								T=1	Sr <sup>[5]</sup> or P
	...								T=1	
	Data								T=1	
	PEC								T=0 <sup>[4]</sup>	

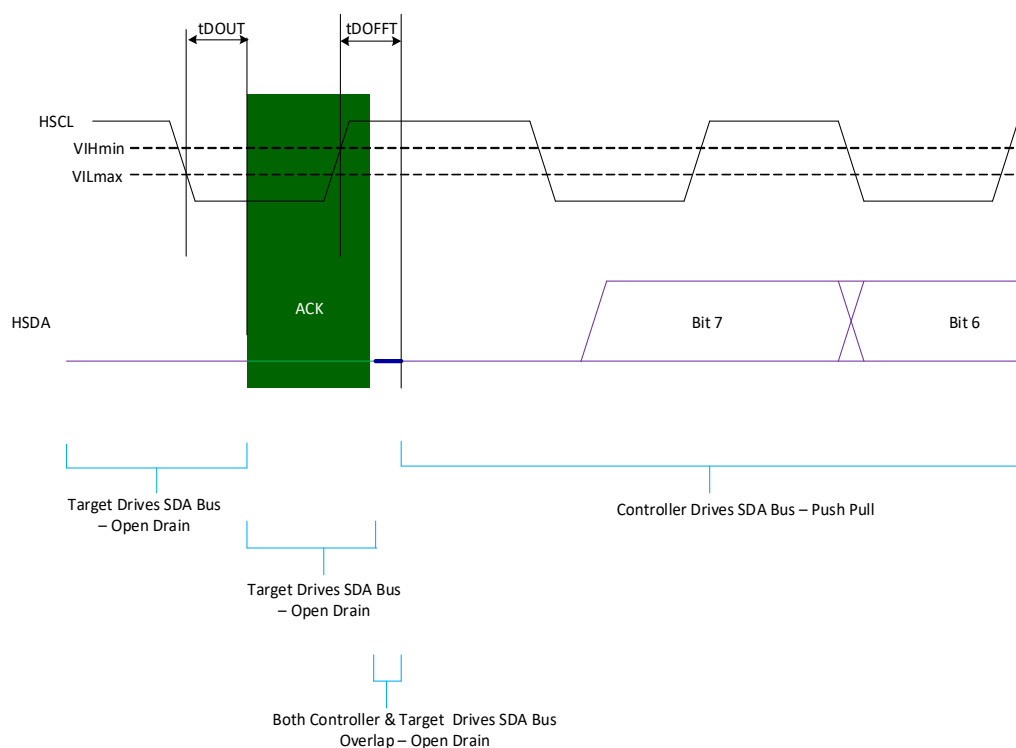
NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Repeat Start).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 See Figure 33 to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

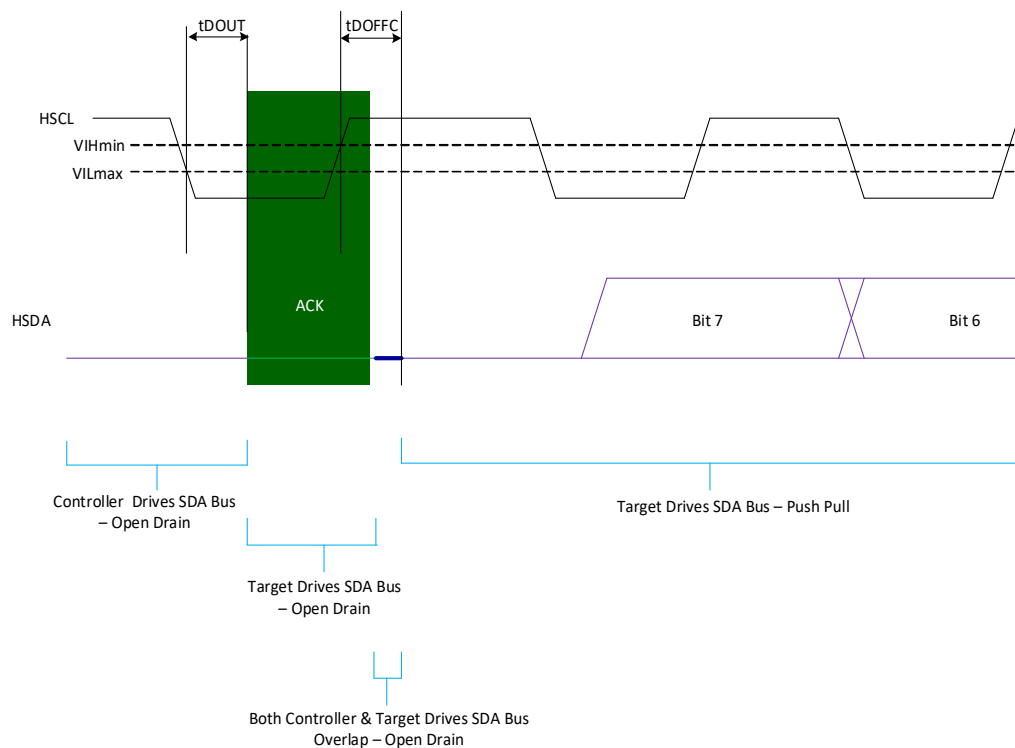
NOTE 4 See Figure 35 to see how Host ends target device operation followed by Host STOP operation.

NOTE 5 Repeat Start or Repeat Start with 7'h7E.



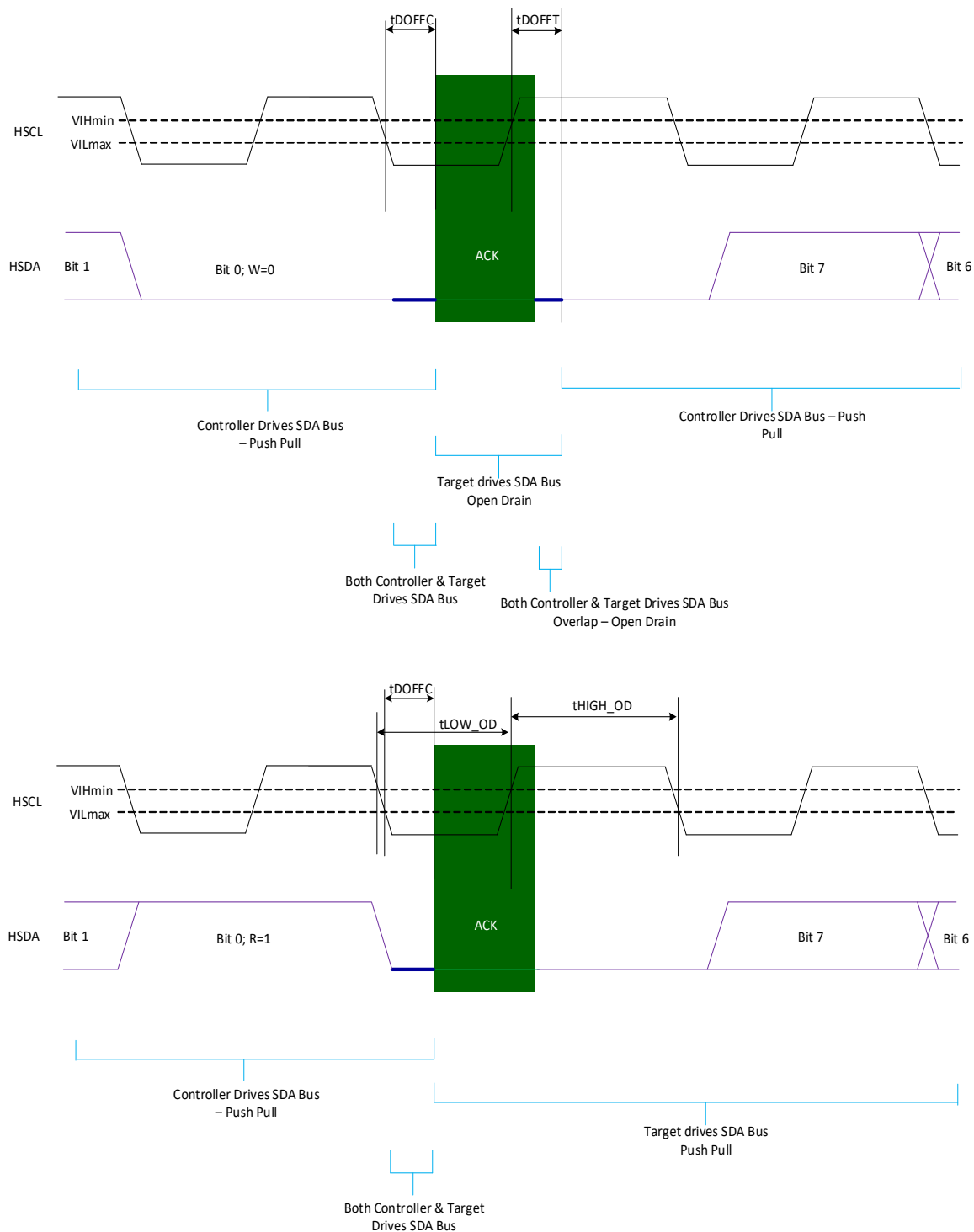
**Figure 31 — Target Open Drain (ACK) to Controller Push Pull Hand Off Operation**

### 5.4.3 Default Read Address Pointer Mode (cont'd)



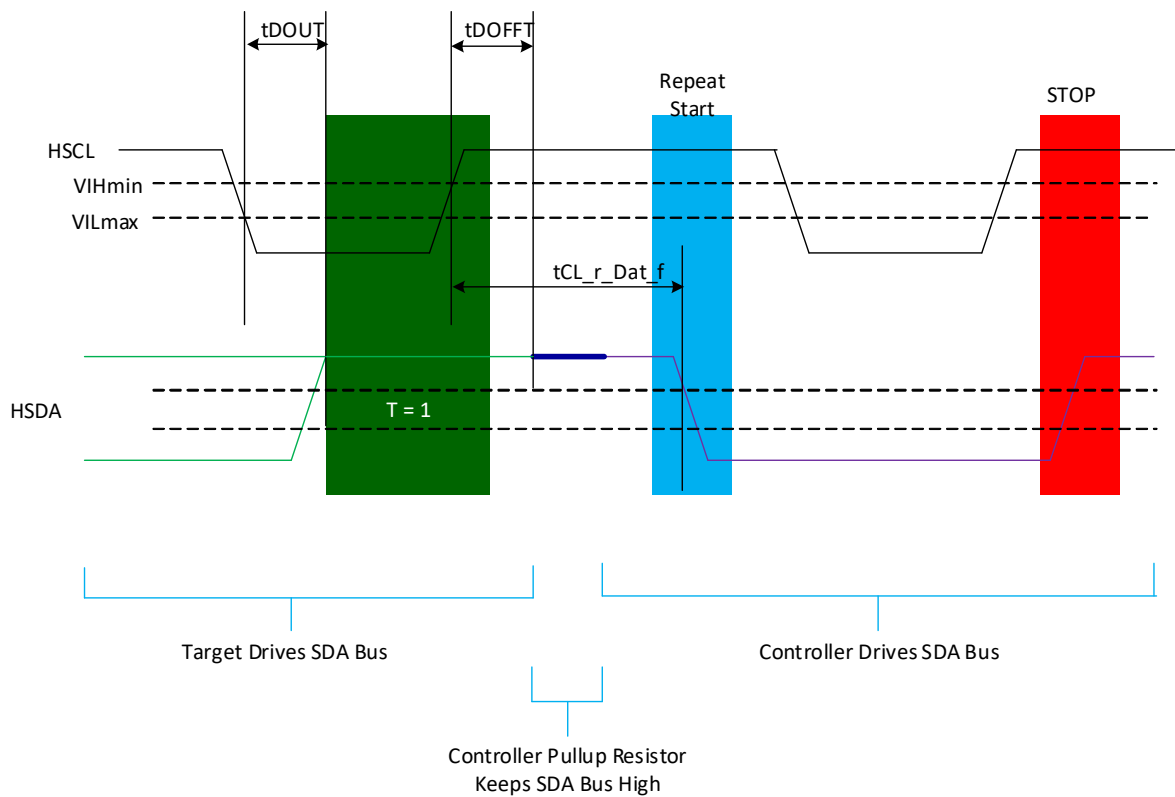
**Figure 32 — Controller Open Drain (ACK) to Target Push Pull Hand Off Operation**

### 5.4.3 Default Read Address Pointer Mode (cont'd)



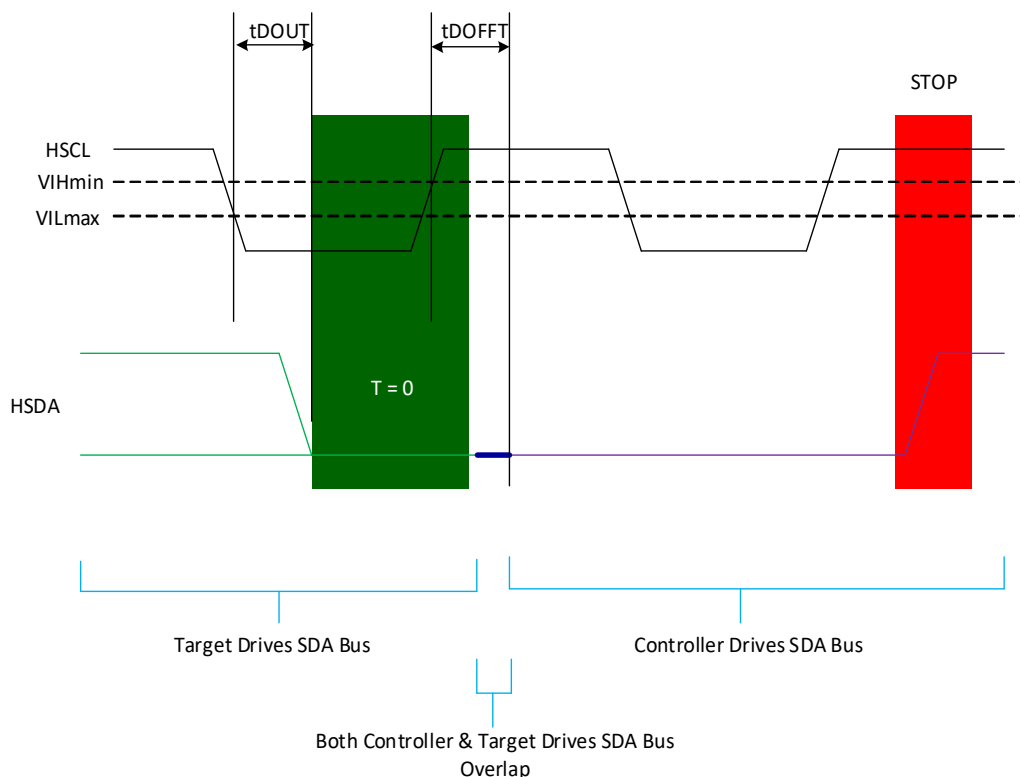
**Figure 33 — Controller Push Pull to Target Open Drain Hand Off Operation**

### 5.4.3 Default Read Address Pointer Mode (cont'd)



**Figure 34 — T=1; Controller Ends Read with Repeated START and STOP Waveform**

### 5.4.3 Default Read Address Pointer Mode (cont'd)



**Figure 35 — T=0; Target Ends Read; Controller Generates STOP**

### 5.4.4 In Band Interrupt (IBI)

In I<sup>2</sup>C mode, in band interrupt function is not supported. Only I3C Basic mode supports in band interrupt function.

The PMIC device supports a feature to enable or disable the event interrupts.

- Interrupt Enable in register [Table 156, Register 0x34 \[6\]](#) - When [Table 156, Register 0x34 \[6\]](#) = '1', the device sends the interrupt at next available opportunity when any of the register bits in [Table 112, Register 0x08 \[7:2,0\]](#), [Table 113, Register 0x09 \[7,5,3:0\]](#), [Table 114, Register 0x0A \[7:2, 0\]](#), [Table 115, Register 0x0B \[7:0\]](#), [Table 155, Register 0x33 \[3:0\]](#), and [Table 173, Register 0x109 \[0\]](#) is set to '1'. The device also sets [Table 114, Register 0x0A \[1\]](#) = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
- When [Table 156, Register 0x34 \[6\]](#) = '0', the device does not send the interrupt regardless of the register bits status in [Table 112, Register 0x08 \[7:2,0\]](#), [Table 113, Register 0x09 \[7,5,3:0\]](#), [Table 114, Register 0x0A \[7:2,0\]](#), [Table 115, Register 0x0B \[7:0\]](#), [Table 155, Register 0x33 \[3:0\]](#) and [Table 173, Register 0x109 \[0\]](#). However, the device does set [Table 114, Register 0x0A \[1\]](#) = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

#### 5.4.4.1 Mechanics of In Band Interrupt Generation

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt (i.e., [Table 114, Register 0x0A](#) [1] = '1') and [Table 156, Register 0x34](#) [6] = '1', the PMIC will request an interrupt after detecting a START condition by transmitting its 7-bit binary address (LID bits of followed by HID bits) followed by R/W bit = '1' on the SDA bus serially (synchronized by SCL falling transitions).

If the PMIC detects no START condition but if the I3C Basic bus (SDA and SCL) has been inactive (no edges seen) for  $t_{\text{AVAL}}$  period, then PMIC may assert SDA low  $t_{\text{IBI\_ISSUE}}$  time to request an interrupt. When the PMIC device requests an interrupt, the Host toggles the SCL. The PMIC transmits its 7-bit binary address; '1001' (LID) followed by '111' (HID) followed by R/W bit = '1'.

When the PMIC requests an interrupt, the host may take one of the two actions below:

- The Host sends ACK on 9<sup>th</sup> bit to accept the interrupt request. At this point, if the PMIC confirms that it has won the arbitration, the PMIC transmits the IBI payload as shown in [Table 60](#) and [Table 61](#) for PEC disabled and PEC enabled configuration respectively. See [Figure 36](#). [Figure 36](#) just shows only first two data bits of the first payload byte (MDB Byte) to illustrate the timing. The interrupt payload contains MDB followed by PMIC error register contents [Table 112, Register 0x08](#) to [Table 115, Register 0x0B](#), [Table 155, Register 0x33](#) and [Table 173, Register 0x109](#) in order. The host then issues the STOP command. Note the timing waveform in [Figure 36](#). The host then accepts the IBI payload if it sends an ACK on 9<sup>th</sup> bit to accept the interrupt request. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the PMIC Hub device retains the IBI Status flag [Table 114, Register 0x0A](#) [1] and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the PMIC device successfully transmits the entire IBI payload, it then clears the IBI Status flag [Table 114, Register 0x0A](#) [1] = '0' and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is an another different event occurs; for another same event, the device does not request for an IBI.
- The Host sends NACK on the 9<sup>th</sup> bit as shown in [Figure 37](#) followed by a STOP command. In this case, the PMIC does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which device sent the IBI request. The PMIC retains the IBI Status flag [Table 114, Register 0x0A](#) [1] = '1' and Pending Interrupt Bits [3:0] = '0001'.

**Table 60 — IBI Payload Packet; PEC is Disabled**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	X	0	X	HID			R=1	A <sup>[1]</sup>	
	MDB = 0x00								T=1	
	R08 [7:0]								T=1	
	R09 [7:0]								T=1	
	R0A [7:0]								T=1	
	R0B [7:0]								T=1	
	R33 [7:0]								T=1	
	R109 [7:0]								T=0 <sup>[2]</sup>	P

NOTE 1 See [Figure 32](#) to see how the transition occurs from Controller Open Drain (ACK) to Target Push Pull operation (1st bit of MDB Byte bit [7])

NOTE 2 See [Figure 35](#) to see how Host ends target device operation followed by Host STOP operation.

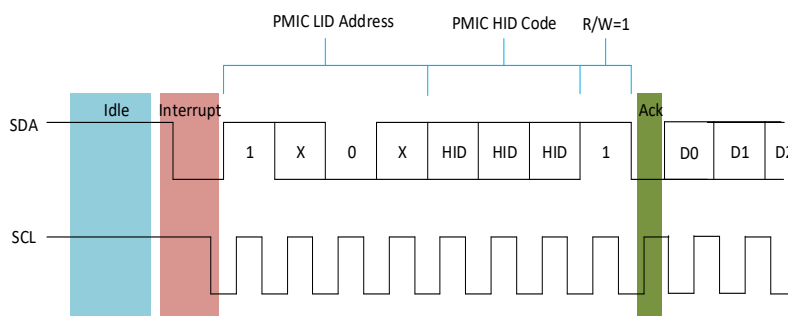
#### 5.4.4.1 Mechanics of In Band Interrupt Generation (cont'd)

**Table 61 — IBI Payload Packet; PEC is Enabled**

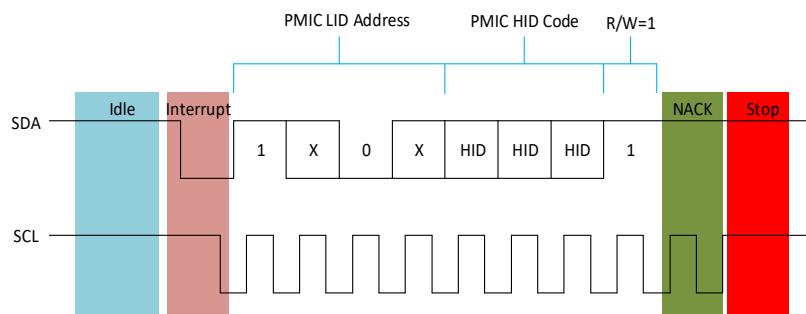
Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/T	Stop
S	1	X	0	X	HID			R=1	A <sup>[1]</sup>	
	MDB = 0x00								T=1	
	R08 [7:0]								T=1	
	R09 [7:0]								T=1	
	R0A [7:0]								T=1	
	R0B [7:0]								T=1	
	R33 [7:0]								T=1	
	R109 [7:0]								T=1	
	PEC								T=0 <sup>[2]</sup>	P

NOTE 1 See Figure 32 to see how the transition occurs from Controller Open Drain (ACK) to Target Push Pull operation (1st bit of MDB Byte bit [7])

NOTE 2 See Figure 35 to see how Host ends target device operation followed by Host STOP operation.



**Figure 36 — PMIC Request Interrupt; Host Ack followed by PMIC IBI Payload**



**Figure 37 — PMIC Requests Interrupt; Host NACK followed by STOP**

#### 5.4.4.2 Interrupt Arbitration

As there are multiple devices I3C bus, multiple devices may request an interrupt when the Host I3C Basic bus is inactive for  $t_{\text{AVAIL}}$  period. Arbitration process is required.

For CAMM2 application environment, there could be up to a total of 13 different devices, including the PMIC on I3C Basic bus.

On a typical CAMM2 application environment, all devices have the same 3-bit HID code. Hence, the arbitration is always won by the lowest 4-bit LID code. For example, if one local target device has LID code of '0010' and the other device (PMIC) has a LID code of '1001', through the arbitration process, the LID code of '0010' wins. The other device (PMIC) with a LID code of '1001' must release the bus and wait for next opportunity to request an interrupt. Table 62 shows the arbitration priority based on the LID code for all devices. The Green colored cells in Table 62 are the likely devices that will be on a standard CAMM2. The Olive colored cells in Table 62 do not apply.

**Table 62 — Interrupt Arbitration - Among All Devices**

Device	LID Code	HID Code = '111'	Arbitration Priority
N/A	0000	N/A	N/A
RFU	0001	111	1
TS0	0010	111	2
RFU	0011	111	3
RFU	0100	111	4
RFU	0101	111	5
TS1	0110	111	6
RFU	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD Hub	1010	N/A	N/A
RCD	1011	111	10
PMIC2	1100	111	11
RFU	1101	111	12
RFU	1110	111	13
N/A	1111	N/A	N/A

An uncommon but possible scenario would be that, at the exact same time as when the Hub or local target devices (i.e., PMIC) are requesting an interrupt, the host is starting an operation to the hub or local target devices (i.e., PMIC). When this happens, Host also gets involved in the arbitration process along with the Hub or the local target devices (PMIC). During the arbitration phase, there will always be only one winning device and it could be either the Hub or the local target device (i.e., PMIC) or the Host.

If the host wins during the arbitration phase, it continues with normal operation. The losing Hub or local target device (i.e., PMIC) waits for next opportunity to send an interrupt.

If the host loses during the arbitration phase, the host must let go of the bus. When Host loses during the arbitration, the host must let the Hub or local target device (i.e., PMIC) finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9<sup>th</sup> bit, the host has two options to take the action as noted below:

- Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning Hub or local target device (i.e., PMIC). After the IBI payload, the host issues STOP operation.



#### 5.4.4.2 Interrupt Arbitration (cont'd)

- Host sends a NACK followed by STOP operation.

A rare but still possible scenario would be that, at the exact same time as when the PMIC is requesting an interrupt, the host is starting an operation to the same PMIC. When this happens, neither Host nor the PMIC knows it is a winner until the 8<sup>th</sup> bit and Host always wins. This is because the PMIC sends R=1 (8<sup>th</sup> bit) during the interrupt. The host sets W=0 (8<sup>th</sup> bit) during the operation. As a result, the host wins and the PMIC must let go of the bus and wait for the next opportunity to send an interrupt.

An extremely rare but still possible scenario would be that, at the same exact time as when PMIC device is requesting an interrupt, the host is requesting a read operation with the default read address pointer mode to the PMIC device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the PMIC device sends R=1 (8<sup>th</sup> bit) during the interrupt and Host also sends R=1 for read request with default read address pointer mode. As a result, there is no winner because Host is waiting for PMIC to ACK and PMIC is waiting for Host to ACK. In this case, neither Host nor PMIC will ACK. Since there is no ACK (i.e., NACK) by either device, the Host must time out and repeat the read request with Repeat Start. When Host repeats the read request with Repeat Start, the PMIC does not send an interrupt because of Repeat Start.

#### 5.4.4.3 Clearing IBI Status and Device Status Registers

The PMIC device provides the IBI status in [Table 114, Register 0x0A \[1\]](#) by setting it to '1'. The PMIC device clears the IBI status register [Table 114, Register 0x0A \[1\]](#) to '0' automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits [3:0] to '0000'. Once IBI status register is cleared, the PMIC does not request for an IBI again unless another event occurs.

The device status registers ([Table 112, Register 0x08 \[6:2,0\]](#), [Table 113, Register 0x09 \[7,5,3:0\]](#), [Table 114, Register 0x0A \[7:2,0\]](#), [Table 115, Register 0x0B \[7:0\]](#), [Table 155, Register 0x33 \[2:0\]](#), and [Table 173, Register 0x109 \[0\]](#)) are latched and remains set even after PMIC device sends IBI payload and clears the IBI status register [Table 114, Register 0x0A \[1\]](#) to '0'. The host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global clear command.

After the host issues a clear command, if the condition is no longer present, the device clears the appropriate status register, clears the IBI status register [Table 114, Register 0x0A \[1\]](#) to '0' and Pending Interrupt Bits [3:0] to '0000' even if the device has not sent the IBI. After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register to [Table 114, Register 0x0A \[1\]](#) '1' and Pending Interrupt Bits [3:0] to '0001' even if the device has already sent the IBI and entire IBI payload.

#### 5.4.5 Packet Error Check Function

In I<sup>2</sup>C mode, packet error checking is not supported. Only I<sup>3</sup>C Basic mode supports packet error checking.

The PMIC device implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PEC is enabled through DEVCTRL CCC. The PEC is a CRC-8 value calculated on all the messages bytes except for START, REPEAT START, STOP conditions or T-bits, ACK, NACK and IBI header (7'h7E followed by W=0) bits.

The polynomial for CRC-8 calculations is:

$$C(X) = X^8 + X^2 + X^1 + 1$$

The seed value for PEC function is all zeros.

When Host calculates PEC for PMIC device, it includes LID and HID bits followed by R/W bit.

### 5.4.6 Parity Error Check Function

In I<sup>2</sup>C mode, parity error checking is not supported except for supported CCCs. Only I3C Basic mode supports parity error checking.

By default, when PMIC device is put in I3C mode, parity function is automatically enabled. The host can disable the function after it is enabled. The host can also disable the parity function with DEVCTRL CCC. When parity function is disabled, the PMIC simply ignores the “T” bit information from the Host. The host may actually choose to compute the parity and send that information during “T” bit or simply drive static low or high in “T” bit.

The PMIC device implements ODD parity. If an odd number of bits in the byte are ‘1’, the parity bit value is ‘0’. If even number of bits in the byte are ‘1’, the parity bit value is ‘1’. The host computes the parity and sends during “T” bit.

### 5.4.7 Packet Error Check and Parity Error Handling

There are two types of error checking done by the PMIC device - Parity error checking and Packet Error checking. By default, the parity error checking is always enabled and packet error checking is disabled. The host may enable the packet error checking at any time. The parity error is calculated for each byte. The host sends parity error information in “T” bit.

I3C basic defines TE0, TE1, TE2, TE3, TE4, TE5, and TE6 error detections for target devices. Only TE1 and TE2 error detections are supported by the PMIC for parity checking. All other errors are not supported and not applicable.

#### 5.4.7.1 Write Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host as shown in [Table 63](#).

**Table 63 — Write Command Data Packet; PEC Disabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A <sup>[1],[2],[3]</sup>	
	Address [7:0]								T	
	Data								T	
	...								T	
	Data								T	

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write Command - if no parity error:

- The PMIC device executes the command.

Write Command - if parity error:

- The PMIC device discards the byte in the packet that had parity error.

#### 5.4.7.1 Write Command Data Packet Error Handling - PEC Disabled (cont'd)

- The PMIC device discards all subsequent bytes in that packet until STOP operation. The PMIC device may or may not check the parity for all subsequent bytes in that packet.
- Note that, as the packet contains more than one byte, if first byte had no parity error but the second byte had a parity error, the PMIC device may or may not execute the first byte operation but second byte and all subsequent bytes operations are discarded.
- The PMIC device sets the register [Table 114, Register 0x0A \[2:1\]](#) to '11'; P\_Err in GETSTATUS CCC to '1'; updates Pending Interrupts Bits [3:0] to '0001'; asserts GSI\_n pin if enabled and waits for the next opportunity to send in band interrupt if IBI is enabled.

#### 5.4.7.2 Read Command Data Packet Error Handling - PEC Disabled

The PMIC device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in [Table 64](#).

The PMIC device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes that PMIC device sends. The PMIC device sends Continuous ('1') or Stop ('0') information during "T" bit when PMIC device is sending the read data.

**Table 64 — Read Command Data Packet; PEC Disabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A <sup>[1].[2].[3]</sup>	
	Address [7:0]								T	
Sr	1	X	0	X	HID			R=1	A/N <sup>[4].[5]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1 <sup>[6].[7]</sup>	Sr <sup>[8]</sup> or P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to parity error, it will always NACK regardless of how many times the host tries Repeat Start. If there were no parity errors, the device may eventually ACK.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 34](#) to see how Host ends target device operation.

NOTE 7 When PMIC device reaches last byte within the region (either Host region or CAMM2 Vendor region), it will continue to return data but returned data will be 0x00 if there is no valid password for CAMM2 Vendor region or Vendor Specific region. Once the address counter reaches 0x1FF, it will reset to address 0x00 and it will continue to return the data. Only host can perform the STOP operation.

NOTE 8 Repeat Start or Repeat Start with 7'h7E.

Read Command - If no parity error:

- The PMIC sends ACK back to the host when Host performs a Repeat Start operation.
- The PMIC device executes the command and sends the data as shown in [Table 64](#).

### 5.4.7.2 Read Command Data Packet Error Handling - PEC Disabled (cont'd)

Read Command - If parity error:

- The PMIC device discards the one byte in the packet that had a parity error.
- The PMIC sends NACK back to the host when Host performs a Repeat Start operation. This is shown in the RED colored cell in Table 64. The NACK represents either a parity error in one byte that it receives from the host or that PMIC is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. If the PMIC device NACKs due to a parity error, it will always NACK regardless of how many times the host tries Repeat Start.
- The PMIC does not send the data shown in Table 64 and instead expects Host to perform STOP operation.
- The PMIC device sets Table 114, Register 0x0A [2:1] to '11'; P\_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI\_n pin if enabled, and waits for the next opportunity to send an in band interrupt if IBI is enabled.

### 5.4.7.3 Write Command Data Packet Error Handling - PEC Enabled

The PMIC device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host as shown in Table 65. Further, the PMIC device checks for the packet error for the entire packet (from Start condition until last byte of Data) that it receives from the host as shown in Table 65.

**Table 65 — Write Command Data Packet; PEC Enabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1],[2],[3]	
	Address [7:0]								T	
	CMD			W=0	0	0	0	0	T	
	Data								T	
	...								T	
	Data								T	
	PEC								T	Sr[4] or P

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 Repeat Start or Repeat Start with 7'h7E.

Write Command - if no parity error:

- The PMIC device waits for the entire packet. If no error in packet, the PMIC device executes the command. If there is an error in the packet, the PMIC device discards the entire packet and does not execute that packet and waits for STOP, sets the Register Table 114, Register 0x0A [3,1] to '11'; PEC\_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI\_n pin enabled, and waits for the next opportunity to send in band interrupt if IBI is enabled.

### 5.4.7.3 Write Command Data Packet Error Handling - PEC Enabled (cont'd)

Write Command - if parity error:

- The PMIC device discards that byte and the entire packet until STOP operation.
- The PMIC device sets the [Table 114, Register 0x0A \[2:1\]](#) to '11'; P\_Err in GETSTATUS CCC to '1'; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI\_n pin if enabled, and waits for the next opportunity to send in band interrupt if IBI is enabled.
- The PMIC may or may not check the error for the packet. If the device checks for the packet error, likely it will detect an error in the packet and the device may also set the [Table 114, Register 0x0A \[3\]](#) and PEC\_ERR in GETSTATUS CCC as well.

### 5.4.7.4 Read Command Data Packet Error Handling - PEC Enable

The PMIC device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in [Table 66](#).

The PMIC device does not compute the parity when it sends the data to the Host. The Host does not check for parity error for the bytes shown in [Table 66](#). The PMIC device sends Continuous ('1') or Stop ('0') information during "T" bit when PMIC device is sending the read data.

The PMIC device checks for the PEC error for a packet that it receives from the Host from Start condition to Repeat Start condition (from first device select code followed by the address offset and CMD byte).

The PMIC device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data PMIC device transmits back to Host).

**Table 66 — Read Command Data Packet; PEC Enabled; 1 Byte Address Mode**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	X	0	X	HID			W=0	A[1],[2],[3]	
	Address [7:0]								T	
	CMD			R=1	0	0	0	0	T	
	PEC								T	
Sr	1	X	0	X	HID			R=1	A/N <sup>[4],[5]</sup>	
	Data								T=1	
	...								T=1	
	Data								T=1	
	PEC								T=0 <sup>[6]</sup>	

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull operation (Address bit 7).

NOTE 2 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 3 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP or next Repeat Start operation.

NOTE 4 If PMIC device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If PMIC device NACKs due to PEC error or parity error, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the PMIC device only includes device select code of the ACK response of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes device select of only the last Repeat Start from the host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.

NOTE 5 See [Figure 33](#) to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).

NOTE 6 See [Figure 35](#) to see how Host ends target device operation followed by Host STOP operation.

NOTE 7 Repeat Start or Repeat Start with 7'h7E.

#### 5.4.7.4 Read Command Data Packet Error Handling - PEC Enable (cont'd)

Read command - If no parity error and no PEC error:

- The PMIC sends ACK back to the host when Host performs a Repeat Start operation.
- The PMIC device executes the command and sends the data as shown in [Table 66](#).
- The PMIC computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) as shown in [Table 66](#).

Read command - if parity or PEC error:

- The PMIC device discards the byte in the packet that had a parity error.
- The PMIC device discards second byte in that packet if a parity error occurred in first byte. The PMIC device may or may not check parity for the second byte in that packet.
- The PMIC device discards the packet if there is a PEC error.
- The PMIC sends NACK back to the host when Host performs Repeat Start operation. This is shown in [RED colored](#) cell in [Table 66](#). The NACK represents either PEC error or parity error in one of the two bytes or that PMIC is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times as it may desire. The PEC calculation by PMIC device only includes device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the PMIC device includes the device select code of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the PMIC device NACKs due to PEC error or parity error in previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.
- The PMIC does not send any data shown in [Table 66](#) and instead expects Host to perform STOP operation.
- The PMIC device sets [Table 114, Register 0x0A \[3:2\]](#) accordingly and [Table 114, Register 0x0A \[1\]](#) to '1'; P\_Err, PEC\_Err in GETSTATUS CCC to '1' accordingly; updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to '0001'; asserts GSI\_n pin if enabled and waits for the next opportunity to send an in band interrupt if IBI is enabled.

#### 5.4.8 CCC Packet Error Handling

Parity error and PEC error detected in a CCC packet are handled the same way as described for normal Read/Write operations.

#### 5.4.9 Error Reporting

All error conditions detected by the PMIC devices are captured in [Table 112, Register 0x08](#) to [Table 115, Register 0x0B](#) and [Table 155, Register 0x33](#) registers.

There are four different possible ways error information can be communicated to the host.

1. The host makes the read request to [Table 112, Register 0x08](#) to [Table 115, Register 0x0B](#) and [Table 155, Register 0x33](#) registers.
2. The host starts any transaction with Start condition followed by 7'h7E IBI header if IBI is enabled (Only applicable in I3C Basic mode).
3. The PMIC device sends in band interrupt if enabled, when its SCL and SDA input has been idle for  $t_{AVAL}$  time.
4. The PMIC asserts GSI\_n pin if enabled.

#### 5.4.10 I3C Basic Common Command Codes (CCC)

The I3C Basic spec lists large number of Common Command Codes (CCC). Not all CCC are required to be supported. The PMIC device NACKs for all unsupported CCC. The PMIC supports CCC as listed in [Table 67](#).

The host shall not access any device specific registers or issue any CCC after VR Enable command (i.e., [Table 154, Register 0x32](#) [6] = '1' or VR\_EN pin asserted high) until tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied.

The PMIC device requires STOP operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address Pointer mode operation must be followed by STOP operation before continuing to any CCC operation. The PMIC device also requires STOP operation between any direct CCC to broadcast CCC.

The PMIC device does allow Repeat Start operation between any direct CCC to any other direct CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

**Table 67 — PMIC CCC Support Requirement**

CCC	Mode	Code	Description	Note
ENEC	Broadcast	0x00	Enable Event Interrupts	
	Direct	0x80		
DISEC	Broadcast	0x01	Disable Event Interrupts	
	Direct	0x81		
RSTDAA	Broadcast	0x06	Put the device in I <sup>2</sup> C Mode (aka: Reset Dynamic Address Assignment)	
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (aka: Set All Addresses to Static Address)	
GETSTATUS	Direct	0x90	Get Device Status	
DEVCAP	Direct	0xE0	Get Device Capability	[1]
SETHID	Broadcast	0x61	PMIC updates its 3-bit HID Code register	1
DEVCTRL	Broadcast	0x62	Configure SPD Hub and all devices behind Hub	1

NOTE 1 JEDEC specific CCC.

##### 5.4.10.1 ENEC CCC

The ENEC CCC is only supported after device is put in I3C Basic mode. In I<sup>2</sup>C mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. When ENEC CCC is registered by the PMIC, it updates [Table 156, Register 0x34](#) [6] = '1' and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 68](#) to [Table 71](#) show examples of ENEC CCC. [Table 72](#) shows the encoding definition for ENEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.



## 5.4.10.1 ENEC CCC (cont'd)

Table 68 — ENEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 69 — ENEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

Table 70 — ENEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W=0	A <sup>1,[2]</sup>	
	0x00							ENINT	T	

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.



#### 5.4.10.1 ENEC CCC (cont'd)

**Table 71 — ENEC CCC - Direct with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A <sup>1,[2]</sup>	
	0x00							ENINT	T	
	PEC								T	Sr <sup>[3]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

**Table 72 — ENEC CCC Byte Encoding**

Bit	Encoding	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal for Host to issue ENEC CCC with ENINT bit = '0'; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset

#### 5.4.10.2 DISEC CCC

The DISEC CCC is only supported after device is put in I3C Basic mode. In I<sup>2</sup>C mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. When DISEC CCC is registered by the PMIC, it updates [Table 156, Register 0x34](#) [6] = '0' and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 73](#) and [Table 75](#) show an example of a single DISEC CCC. [Table 77](#) shows the encoding definition for DISEC CCC.

In I3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

**Table 73 — DISEC CCC - Broadcast**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

**5.4.10.2 DISEC CCC (cont'd)****Table 74 — DISEC CCC - Broadcast with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x01 (Broadcast)								T	
	7'h00							DISINT	T	
	PEC								T	
										Sr <sup>[2]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

**Table 75 — DISEC CCC - Direct**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W=0	A <sup>1,[2]</sup>	
	0x00							DISINT	T	
										Sr <sup>[3]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

**Table 76 — DISEC CCC - Direct with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A <sup>1,[2]</sup>	
	0x00							DISINT	T	
	PEC								T	
										Sr <sup>[3]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 The PMIC device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The PMIC device ignores the entire packet until STOP operation or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

#### 5.4.10.2 DISEC CCC (cont'd)

**Table 77 — DISEC CCC Byte Encoding**

Bit	Encoding	Notes
DISINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal for Host to issue DISEC CCC with DISINT bit = '0'; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset

#### 5.4.10.3 RSTDAA CCC

The RSTDAA CCC is only supported after device is put in I3C Basic mode. In I<sup>2</sup>C mode, this CCC is ignored (i.e., the RSTDAA command is not executed internally and any bytes arriving after the 0x06 RSTDAA Broadcast CCC are ignored for all purposes, including parity checking, until the next STOP operation or Repeat START with 7'h7E is received). When RSTDAA CCC is registered by the PMIC, it updates [Table 152, Register 0x30 \[2\] = '0'](#), [Table 154, Register 0x32 \[6\] = '0'](#), it disables PEC and IBI function ([Table 156, Register 0x34 \[7:6\] = '00'](#)), and clears parity function [Table 156, Register 0x34 \[5\] = '0'](#)) and it takes in effect at the next Start operation (i.e., after STOP operation).

[Table 78](#) and [Table 79](#) show an example of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

**Table 78 — RSTDAA CCC - Broadcast**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x06 (Broadcast)								T	P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

**Table 79 — RSTDAA CCC - Broadcast with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x06 (Broadcast)								T	
	PEC								T	P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

#### 5.4.10.4 SETAASA CCC

The SETAASA CCC is only supported when device is in I<sup>2</sup>C mode. In I<sup>2</sup>C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any parity error the host shall limit the maximum speed of operation for this CCC to 1 MHz. In I3C Basic mode, this CCC is ignored (i.e., the SETAASA CCC is not executed internally). When SETAASA CCC is registered by the PMIC, it updates [Table 154, Register 0x32 \[6\] = '1'](#) and it takes in effect at the next Start operation (i.e., after STOP operation). [Table 80](#) shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I<sup>2</sup>C mode and there is no PEC function in I<sup>2</sup>C mode.

**5.4.10.4 SETAASA CCC (cont'd)****Table 80 — SETAASA CCC - Broadcast**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

**5.4.10.5 GETSTATUS CCC**

The GETSTATUS CCC is supported in I3C Basic mode. In I<sup>2</sup>C mode, this CCC is ignored (i.e., it is not executed internally and the Repeat Start byte arriving after the 0x90 GETSTATUS CCC code is not acknowledged and host must do STOP operation). [Table 81](#) to [Table 82](#) show an example of a single GETSTATUS CCC.

In I3C mode only, if PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

**Table 81 — GETSTATUS CCC - Direct**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x90 (Direct)								T	
Sr	DevID[6:0]								R=1	
	PEC_Err	0	0	0	0	0	0	0	T=1	
	0	0	P_Err	0	Pending Interrupt				T=0	Sr <sup>[2]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

**Table 82 — GETSTATUS CCC - Direct with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	Sr <sup>[2]</sup> or P
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A <sup>1</sup>	
	PEC_Err	0	0	0	0	0	0	0	T=1	
	0	0	P_Err	0	Pending Interrupt				T=1	
	PEC								T=0	

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

#### 5.4.10.5 GETSTATUS CCC (cont'd)

**Table 83 — GETSTATUS CCC Byte Encoding**

Bit	Encoding	Notes
PEC_Err	0 = No Error 1 = PEC Error Occurred	This register is cleared when Host issues clear command to <a href="#">Table 122, Register 0x12</a> [3]
P_Err	0 = No Error 1 = Protocol Error; Parity Error Occurred	This register is cleared when Host issues clear command to <a href="#">Table 122, Register 0x12</a> [2].
Pending Interrupt	0000 = No Pending Interrupt or No New Global Status Event 0001 = Pending Interrupt or New Global Status Event All other encodings are reserved	This register is cleared when Host issues clear command to any appropriate device status register that causes IBI Status register to get cleared.

When the PMIC device responds to GETSTATUS CCC, after it completes the response, the PEC\_Err, P\_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command by writing '1' to appropriate status or by issuing Global Clear command. Once device clears the appropriate status register, only then PEC\_Err, P\_Err and Pending Interrupt Bits [3:0] gets cleared.

After host issues clear command, if the condition is still present, the device will again set the appropriate status register, sets the IBI status register [Table 114, Register 0x0A](#) [1] to '1' and Pending Interrupt Bits [3:0] to '0001'.

#### 5.4.10.6 DEVCAP CCC

The DEVCAP CCC is only supported after device is put in I3C Basic mode. In I<sup>2</sup>C mode, it is illegal for host to issue this CCC; the PMIC ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. [Table 84](#) to [Table 85](#) show an example of a single DEVCAP CCC. [Table 86](#) defines the encoding for DEVCAP CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

**Table 84 — DEVCAP CCC - Direct**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0xE0 (Direct)								T	
Sr	DevID[6:0]								R=1	
	MSB (Each bit defines capability)								T=1	
	LSB (Each bit defines capability)								T=0	
										Sr <sup>[2]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

**5.4.10.6 DEVCAP CCC (cont'd)****Table 85 — DEVCAP CCC - Direct with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A <sup>1</sup>	
	MSB (Each bit defines capability)								T=1	
	LSB (Each bit defines capability)								T=1	
	PEC								T=0	Sr <sup>[2]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 Repeat Start or Repeat Start with 7'h7E.

**Table 86 — DEVCAP CCC Byte Encoding**

Bit	Encoding	Notes
MSB [7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	PMIC hard codes this to '1'.
MSB[1:0]	RFU	Coded as '00'
LSB[7:0]	RFU	Coded as '0x00'

**5.4.10.7 SETHID CCC**

The SETHID CCC is supported only when device is in I<sup>2</sup>C mode. In I<sup>2</sup>C mode, when host issues this CCC to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed of operation for this CCC to 1 MHz. In I<sup>3</sup>C Basic mode, it is illegal for host to issue this CCC; the PMIC may ignore it or subsequent PMIC operation may not be guaranteed and the PMIC may require Bus Reset. When SETHID CCC is registered by the PMIC, it updates [Table 156, Register 0x34 \[3:1\]](#) with the HID code received by the PMIC and it takes effect at the next Start operation (i.e., after STOP operation). [Table 87](#) shows an example of a single SETHID CCC. As the device is in I<sup>2</sup>C mode when SETHID CCC is issued, the PEC function is not supported.

Once PMIC receives SETHID CCC and updates its 3-bit HID code, after the Stop operation, PMIC device only responds to updated 7-bit address. The 4-bit LID code of the PMIC device remains as is.

The Host may issue SETHID CCC more than one time.

#### 5.4.10.7 SETHID CCC (cont'd)

**Table 87 — SETHID CCC - Broadcast**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0000				HID			0	T	P

#### 5.4.10.8 DEVCTRL CCC

On a typical I3C bus, there can be up to 120 devices. For CAMM2 application environment, there are up to 8 SPD5 Hub devices and behind each SPD5 Hub devices, there are 4 local target devices totaling up to 40 or more devices on I3C Basic bus. For certain operations such as enable or disable functions that are common to all devices (i.e., Packet Error Check), the host must go through one device at a time, which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported in either I<sup>2</sup>C mode or I3C Basic mode of operation. In I<sup>2</sup>C mode, when host issues this CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed of operation for this CCC to 1 MHz.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

The host must pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (i.e., RegMod = '1'), the host must still follow any device register restrictions. For instance, if any device specific register, such as IO timing parameter related register requires STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

There are additional restrictions that host must pay attention to:

- DEVCTRL CCC must be followed by STOP operation before starting a device specific register access. In other words, host shall avoid DEVCTRL CCC followed by Repeat Start to do a device specific register operation. Note that host is allowed to do multiple DEVCTRL CCC with Repeat Start in between to the same device or across multiple devices.
- DEVCTRL CCC must be followed by STOP operation before starting Default Read Address Pointer Mode even across different devices.

**5.4.10.8 DEVCTRL CCC (cont'd)****Table 88 — DEVCTRL CCC - Broadcast**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T <sup>[2]</sup>	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr <sup>[3]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device select code. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.

**Table 89 — DEVCTRL CCC - Broadcast with PEC**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T <sup>[2]</sup>	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr <sup>[3]</sup> or P

NOTE 1 The PMIC device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

NOTE 2 An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device select code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.

NOTE 3 Repeat Start or Repeat Start with 7'h7E.



#### 5.4.10.8 DEVCTRL CCC (cont'd)

**Table 90 — DEVCTRL CCC Command Definition**

Parameter	Definition
AddrMask[2:0]	<p>Broadcast, Unicast or Multicast Command Selection</p> <p>000 = Unicast Command; PMIC device responds if DevID[6:0] field matches with PMIC device's own 7-bit address (4-bit LID + 3-bit HID)</p> <p>011 = Multicast Command; PMIC device and possible other device responds if DevID[6:3] field matches with PMIC device's own 4-bit LID address</p> <p>111 = Broadcast Command; All devices respond to this command</p> <p>All other encodings are reserved</p>
StartOffset[1:0]	<p>Only applicable if RegMod = '0'</p> <p>Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation.</p> <p>00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3</p>
PEC BL[1:0]	<p>Only applicable if RegMod = '0' and PEC function is enabled.</p> <p>Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes.</p> <p>00 = 1 Byte 01 = 2 Byte 10 = 3 Byte 11 = 4 Byte</p>
RegMod	<p>Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register.</p> <p>0 = Access to General Registers in Byte 0 to Byte 3 (i.e., StartOffset[1:0] = Valid) 1 = Device Specific Offset Address (i.e., StartOffset[1:0] and PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.</p>
DevID[6:0]	<p>Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0].</p> <p>If AddrMask[2:0] = '111', DevID[6:0] is a don't care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.</p>

## 5.4.10.8 DEVCTRL CCC (cont'd)

Table 91 — DEVCTRL CCC Data Payload Definition

Byte #	Bit #	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0 = Disable 1 = Enable	Table 156, Register 0x34 [7] is updated
	[6]	Parity Disable	0 = Enable 1 = Disable	Table 156, Register 0x34 [5] is updated
	[5:2]	RFU	RFU	
	[1]	VR Enable	0 = VR Disable 1 = VR Enable	Table 154, Register 0x32 [7] is updated Only PMIC device responds to this bit. All other device ignore this bit.
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global & IBI Clear	0 = No Action 1 = Clear All Event and pending IBI <sup>[1]</sup>	Table 124, Register 0x14 [0] is updated.
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	

NOTE 1 After target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.

## 5.4.10.8.1 DEVCTRL CCC Examples - RegMod = '0'

Table 92 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of '1001' on I3C bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable parity function. The host sends AddrMask = '011' to indicate Multicast command with DevID[6:3] match; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices with DevID[6:3] that matches to '1001' will do the VR Enable command and DevID[6:3] that matches to '0110' will disable the parity function.

Table 92 — DEVCTRL CCC Example - Multicast Command to '1001' and '0110' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W=0	A <sup>1</sup>	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

#### 5.4.10.8.1 DEVCTRL CCC Examples - RegMod = '0' (cont'd)

Table 93 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices will enable PEC function.

**Table 93 — DEVCTRL CCC Example - Broadcast Command to all Devices**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 94 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unicast command to enable VR on CAMM2. The host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, PMIC on CAMM2 will enable its regulator.

**Table 94 — DEVCTRL CCC Example - Unicast Command to PMIC on CAMM25**

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	

NOTE 1 See Figure 31 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

#### 5.4.10.8.2 DEVCTRL CCC Examples - RegMod = '1'

Table 95 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively followed by all devices with 4-bit LID of '1001' on the I3C Basic bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

## 5.4.10.8.2 DEVCTRL CCC Examples - RegMod = '1' (cont'd)

Table 95 — DEVCTRL CCC Example - Multicast Command to '0010' and '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	0010 000							0	T	
	0001 1100 (address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (data)								T	
	0101 0101 (data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W=0	A <sup>1</sup>	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0101 (address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (data)								T	
	PEC								T	P

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

[Table 96](#) shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 96 — DEVCTRL CCC Example - Multicast Command to '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A <sup>[1]</sup>	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (address offset 0x13)								T	
	1111 1111 (data)								T	
	0000 0001 (data)								T	

NOTE 1 See [Figure 31](#) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

### 5.4.11 IO Operation

At power on, by default, the PMIC device comes up in I<sup>2</sup>C mode of operation with Open Drain IO for its management interface. The maximum speed is limited to 1 MHz and supported IO voltage levels are from 1.0 V to 3.3 V.

After power on, the host may put the interface of the PMIC device in I3C Basic mode of operation.

In I3C Basic mode, the host may drive the SCL clock input of the PMIC device using either Push-Pull output driver or the open-drain output driver. It is expected that for all CAMM2 family environment, the host may always drive the SCL clock input using a Push-Pull output driver.

To support in band interrupt, the PMIC device supports dynamic switching between Open Drain mode and Push Pull mode on its SDA bus for various events. [Table 97](#) describes the different modes of operation by the PMIC device for each cycle in I3C Basic mode.

**Table 97 — PMIC Device Dynamic IO Operation Mode Switching; I3C Basic Mode**

	Open Drain Mode	Push Pull Mode
START + Device Select Code	Yes	No
START + 7'h7E IBI Header Byte	Yes	No
REPEAT START + Device Select Code	No	Yes
REPEAT START + 7'h7E Header Byte	No	Yes
CCC Byte (i.e., after 7'h7E+W=0+ACK)	No	Yes
STOP	No	Yes
ACK/NACK Responses	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

### 5.4.12 Bus Clear

The device supports the following described Bus Clear feature in I<sup>2</sup>C mode only. Any attempt by host to perform I<sup>2</sup>C Bus clear on a target device in I3C mode may result in an active drive bus contention on the SDA data line.

There may be abnormal circumstances when the host abruptly stops clocking SCL while the target device is in the middle of outputting data for read operation. For these types of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually, when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transactions with Start condition.

### 5.4.13 Bus Reset

To prevent a malfunctioning device from locking up the I<sup>2</sup>C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on SCL as shown in [Figure 38](#) to force a device bus reset. All devices on a I<sup>2</sup>C or I3C Basic bus reset simultaneously. Bus reset operation works same way regardless of whether device is operating in I<sup>2</sup>C or I3C Basic mode.

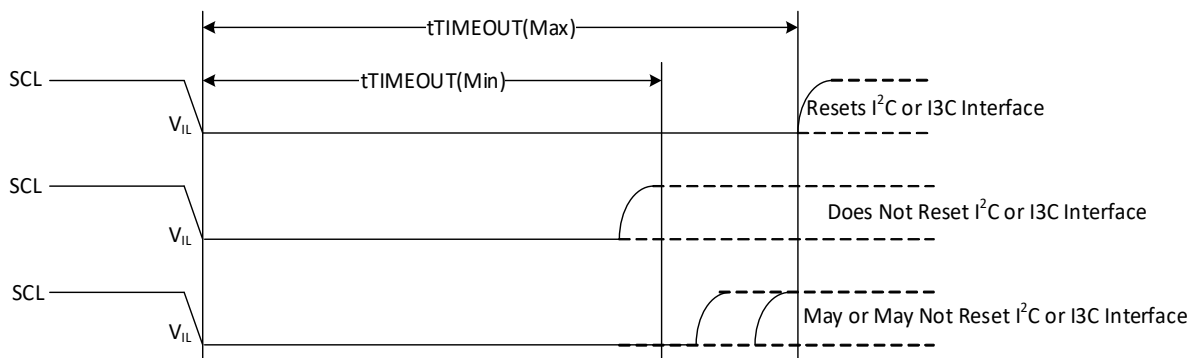
To guarantee the PMIC resets I<sup>2</sup>C bus or I3C Basic bus, the SCL clock input Low time has to be greater than or equal to  $t_{\text{TIMEOUT(Max)}}$ .

The PMIC does not reset I<sup>2</sup>C bus or I3C Basic bus if the SCL clock input Low time is less than  $t_{\text{TIMEOUT(Min)}}$ .

If the SCL clock input Low time is between  $t_{\text{TIMEOUT(Min)}}$  and  $t_{\text{TIMEOUT(Max)}}$ , the PMIC does not guarantee and it may or may not reset the I<sup>2</sup>C bus or I3C Basic bus.

When RESET, the PMIC device takes the following actions:

1. Interface and any pending command or transactions are cleared
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Device returns to I<sup>2</sup>C mode of operation; resets [Table 114, Register 0x0A \[3:2\] = '00'](#); resets [Table 152, Register 0x30 \[2\] = '0'](#); resets [Table 154, Register 0x32 \[6\] = '0'](#); resets [Table 156, Register 0x34 \[7:5\] = '000'](#); and resets [Table 156, Register 0x34 \[3:1\] = '111'](#).
4. Device does not resample PID pin.
5. Device floats the SDA pin such that it gets pulled High by the external or Hub device pullup resistor.
6. Device treats bus reset as STOP operation.



**Figure 38 — I<sup>2</sup>C or I3C Basic Bus Reset of PMIC**

#### 5.4.14 Command Truth Table

The command truth table only applies in I3C mode with PEC enabled for the CMD field (bits [7:5] for Write and Read data packet). In I<sup>2</sup>C mode and in I3C Basic mode with PEC disabled, the command truth table does not apply.

**Table 98 — I3C Basic Mode with PEC Enabled Command Truth Table**

PMIC Command (CMD Field)	Command Name	Command Code	RW	PMIC 8 bit Register Address [7:0]
		2nd Byte Bits [7:5]	2nd Byte Bit [4]	1st Byte Bits [7:0]
Write 1 Byte to Register	W1R	000	0	V
Read 1 Byte from Register	R1R		1	V
Write 2 Byte to Register	W2R	001	0	V
Read 2 Byte from Register	R2R		1	V
Write 4 Byte to Register	W4R	010	0	V
Read 4 Byte from Register	R4R		1	V
Write 16 Byte to Register	W16R	011	0	V
Read 16 Byte from Register	R16R		1	V
Reserved	RSVD	100	RSVD	RSVD
Reserved	RSVD	101	RSVD	RSVD
Reserved	RSVD	110	RSVD	RSVD
Reserved	RSVD	111	RSVD	RSVD

## 6 Schematics

### 6.1 CAMM2 Schematic

Figure 39 shows an example schematic. Table 99 shows all component details shown in the schematics. Note that distributed capacitance across the entire CAMM is not shown in the schematic.

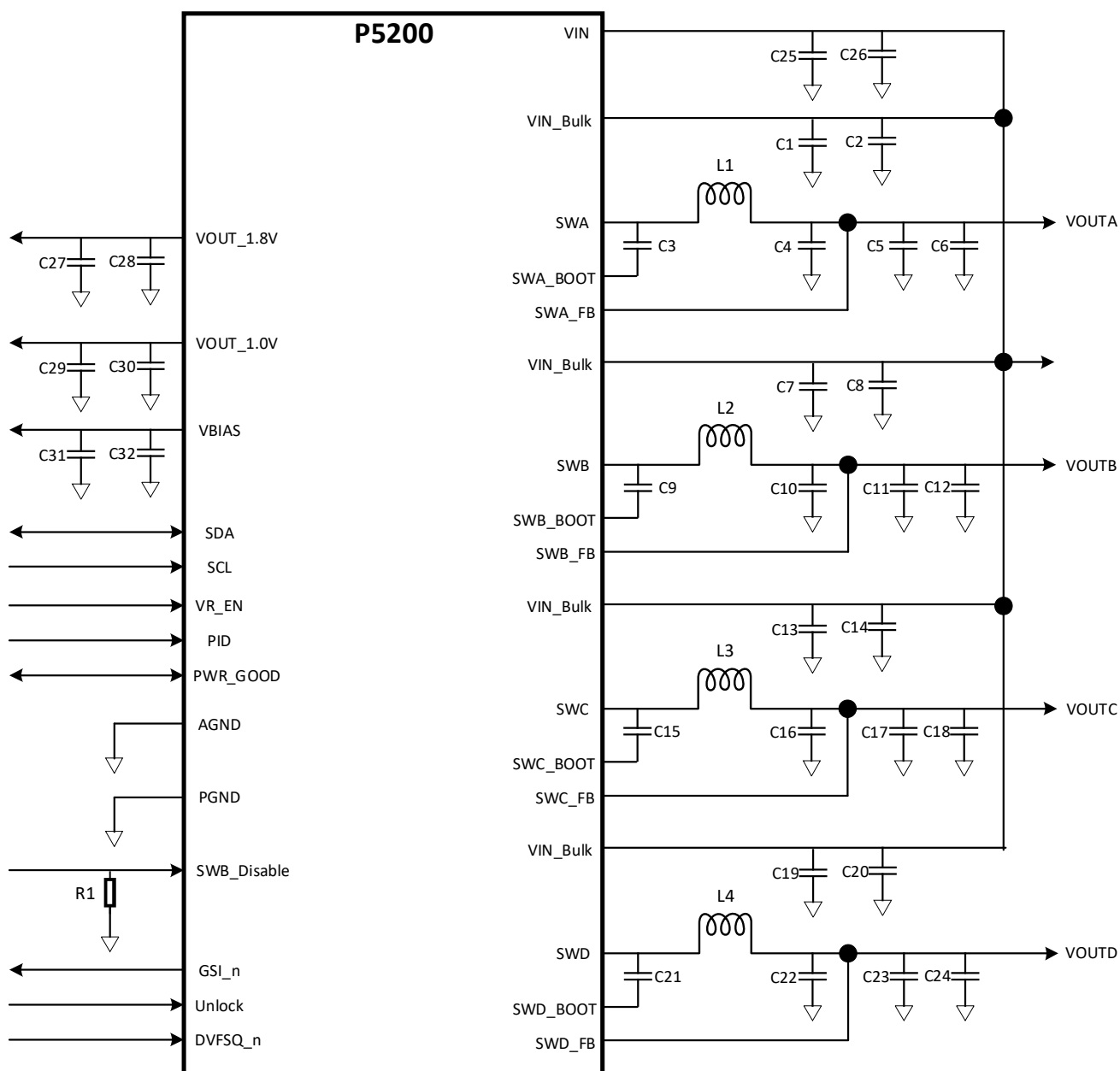


Figure 39 — PMIC5200 Schematic



## 6.1 CAMM2 Schematic (cont'd)

Table 99 — PMIC Schematic Values

Remark	Component	Quantity	Value	Physical Size	Unit	Comment
SWA	L1	1	0.47	4.3 mm x 4.3 mm x 1.2 mm	μH	
SWB	L2	1	1.0	3.4 mm x 2.7 mm x 1.2 mm	μH	
SWC	L3	1	1.5	2.7 mm x 2.2 mm x 1.2 mm	μH	
SWD	L4	1	1.5	2.7 mm x 2.2 mm x 1.2 mm	μH	
SWA	C1	1	0.1	0201; 10V	μF	
	C2	4	22	0603; 10V	μF	
	C3	1	0.1	0201; 10V	μF	
	C4	2	47	0603; 6.3V	μF	
	C5	1	47	0603; 6.3V	μF	
	C6	1	47	0603; 6.3V	μF	
SWB	C7	1	0.1	0201; 10V	μF	
	C8	2	22	0603; 10V	μF	
	C9	1	0.1	0201; 10V	μF	
	C10	1	47	0603; 6.3V	μF	
	C11	1	47	0603; 6.3V	μF	
	C12	1	47	0603; 6.3V	μF	Optional
SWC	C13	1	0.1	0201; 10V	μF	
	C14	2	22	0603; 10V	μF	
	C15	1	0.1	0201; 10V	μF	
	C16	1	47	0603; 6.3V	μF	
	C17	1	47	0603; 6.3V	μF	
	C18	1	47	0603; 6.3V	μF	Optional
SWD	C19	1	0.1	0201; 10V	μF	
	C20	2	22	0603; 10V	μF	
	C21	1	0.1	0201; 10V	μF	
	C22	1	47	0603; 6.3V	μF	
	C23	1	47	0603; 6.3V	μF	
	C24	1	47	0603; 6.3V	μF	Optional
VIN	C25	1	0.1	0201; 10V	μF	
	C26	1	4.7	0402; 10V	μF	
VOUT_1.8V	C27	1	0.1	0201; 6.3V	μF	
	C28	1	4.7	0402; 6.3V	μF	
VOUT_1.0V	C29	1	0.1	0201; 6.3V	μF	
	C30	1	4.7	0402; 6.3V	μF	
VBIAS	C31	1	0.1	0201; 6.3V	μF	
	C32	1	4.7	0402; 6.3V	μF	
SWB_Disable	R1	1	100	0201	KΩ	

## 7 Inductor Specification

### 7.1 Mechanical Specification

The inductor package dimensions and its recommended land patterns are defined in [Figure 40](#) to [Figure 42](#).

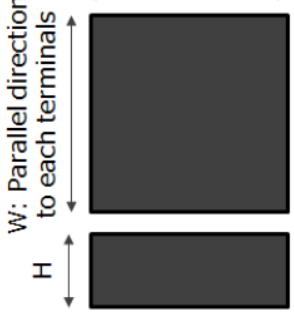
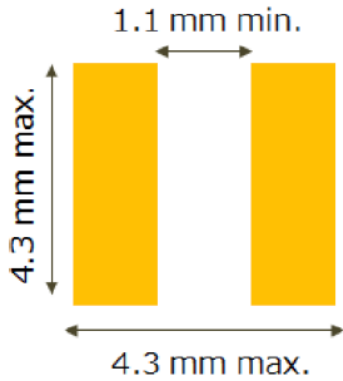
Package Size		Reference Drawing	Recommended Land Pattern
<b>L</b> [mm]	4.3 max	<p>L: Perpendicular direction to each terminals</p>  <p>W: Parallel direction to each terminals</p> <p>H</p> <p>※Not to scale</p>	 <p>1.1 mm min.</p> <p>4.3 mm max.</p> <p>4.3 mm max.</p> <p>※Not to scale</p>
<b>W</b> [mm]	4.3 max		
<b>H</b> [mm]	1.2 max		

Figure 40 — Reference Drawing and Recommended Land Pattern; SWA

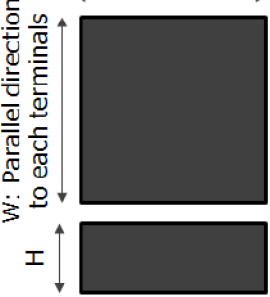
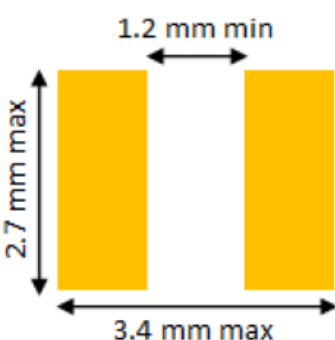
Package Size		Reference Drawing	Recommended Land Pattern
<b>L</b> [mm]	3.4 max	<p>L: Perpendicular direction to each terminals</p>  <p>W: Parallel direction to each terminals</p> <p>H</p> <p>※Not to scale</p>	 <p>1.2 mm min</p> <p>2.7 mm max</p> <p>3.4 mm max</p> <p>※Not to scale</p>
<b>W</b> [mm]	2.7 max		
<b>H</b> [mm]	1.2 max		

Figure 41 — Reference Drawing and Recommended Land Pattern; SWB

7.1 Mechanical Specification (cont'd)

Package Size		Reference Drawing	Recommended Land Pattern
L [mm]	2.7 max	<div>L: Perpendicular direction to each terminals</div> <div>W: Parallel direction to each terminals</div> <div>H</div> <div>※ Not to scale</div>	<div>1.2 mm min</div> <div>2.0 mm max</div> <div>2.8 mm max</div> <div>※ Not to scale</div>
W [mm]	2.2 max		
H [mm]	1.2 max		

Figure 42 — Reference Drawing and Recommended Land Pattern; SWC, SWD

## 7.2 Electrical Specification

The inductor electrical specifications are defined in [Table 100](#) to [Table 102](#).

**Table 100 — Inductor Electrical Specification; SWA<sup>[1]</sup>**

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias ( $\mu$ H)	Max DCR (m $\Omega$ )	Max ACR @ 1 MHz <sup>[2],[3]</sup> (m $\Omega$ )	Min L @ Ipeakmax of <sup>[4]</sup> ( $\mu$ H)
1.2 Max	0.47 $\pm$ 20%	8.5	93	0.24

NOTE1 Test condition: Ambient Temperature = 20  $\pm$  2 <sup>0</sup>C; Ambient Humidity = 65  $\pm$  5% Rh

NOTE2 ACR definition: ACR = Rs @ 1 MHz - DCR. Measured current (1 MHz/sinusoidal): 0.52A rms with no DC Bias for all cases.

NOTE3 For Rs measurement, it is recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments or other instruments which is guaranteed on the measurement accuracy by inductor vendors.

NOTE4 Minimum inductance is defined at DC bias current given by definition in Ipeakmax; [Table 4](#).

**Table 101 — Inductor Electrical Specification; SWB<sup>[1]</sup>**

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias ( $\mu$ H)	Max DCR (m $\Omega$ )	Max ACR @ 1 MHz <sup>[2],[3]</sup> (m $\Omega$ )	Min L @ Ipeakmax of <sup>[4]</sup> ( $\mu$ H)
1.2 Max	1.0 $\pm$ 20%	22	185	0.7

NOTE1 Test condition: Ambient Temperature = 20  $\pm$  2 <sup>0</sup>C; Ambient Humidity = 65  $\pm$  5% Rh

NOTE2 ACR definition: ACR = Rs @ 1 MHz - DCR. Measured current (1 MHz/sinusoidal): 0.13A rms with no DC Bias for all cases.

NOTE3 For Rs measurement, it is recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments or other instruments which is guaranteed on the measurement accuracy by inductor vendors.

NOTE4 Minimum inductance is defined at DC bias current given by definition in Ipeakmax; [Table 6](#).

**Table 102 — Inductor Electrical Specification; SWC, SWD<sup>[1]</sup>**

Package Height (mm)	L @ 0.5-1 MHz; 0 Bias ( $\mu$ H)	Max DCR (m $\Omega$ )	Max ACR @ 1 MHz <sup>[2],[3]</sup> (m $\Omega$ )	Min L @ Ipeakmax of <sup>[4]</sup> ( $\mu$ H)
1.2 Max	1.5 $\pm$ 20%	36	300	1.0

NOTE1 Test condition: Ambient Temperature = 20  $\pm$  2 <sup>0</sup>C; Ambient Humidity = 65  $\pm$  5% Rh

NOTE2 ACR definition: ACR = Rs @ 1 MHz - DCR. Measured current (1 MHz/sinusoidal): 0.22A rms with no DC Bias for all cases.

NOTE3 For Rs measurement, it is recommended to measure by Iwatsu SY-8218 (BH Analyzer, with NF IE-1125B), its upper compatible instruments or other instruments which is guaranteed on the measurement accuracy by inductor vendors.

NOTE4 Minimum inductance is defined at DC bias current given by definition in Ipeakmax; [Table 5](#), and [Table 7](#).

## 8 Registers

### 8.1 Register Attribute Definition

All volatile registers have Base Attributes as defined in [Table 103](#). Some register attributes are further modified with Attribute Modifiers, as defined in [Table 104](#).

**Table 103 — Register Base Attributes**

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Writes have no effect.
Read/Write	RW	This bit can be read or written by host.
Write Only	W	This bit can only be written by host. Read from this bit returns '0'.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return '0' when read. Write has no effect.

**Table 104 — Register Attribute Modifier**

Attribute	Abbreviation	Description
Write 1 Only	1O	This bit can only be set (i.e., write '1') but not reset (i.e., write '0'). Write '0' has no effect.
Protected	P	This bit is protected by the password. This bit cannot be written to unless the password code has been written into the password registers.
Persistent	E	This bit is persistent during power cycle but Erasable with Command.
Persistent	A	This bit is read only persistent register set by PMIC vendor during manufacturing.

### 8.2 Register Map Breakdown

**Table 105 — Register Map Breakdown**

Register Range	Region	Comments
0x00 - 0x3F	Host Region	Host Accessible Registers
0x40 - 0x6F	CAMM2 Vendor Region	<p>CAMM2 Vendor Registers - Non Volatile Memory</p> <p>Allows CAMM2 vendors to program the PMIC for a given DRAM/CAMM2 vendor designs.</p> <p>These are password protected registers and password is selected by CAMM2 vendor. Under normal operation, these registers are not used by any host.</p> <p>These registers require password for read access. Access to these registers without correct password will return all data as '0'.</p> <p>These registers require complete power cycle before it takes effect. Changing these registers under normal operation is considered an illegal operation.</p>
0x70 - 0xFF	Vendor Specific Region	<p>Vendor Specific Registers - Non Volatile Memory</p> <p>These are vendor specific password protected registers. Under normal operation these registers are not used by any host.</p> <p>These registers require password for read access. Access to these registers without correct password will return all data as '0'.</p>
0x100 - 0x13F	Host Region	Host Accessible Registers

### 8.2.1 Memory Protection

The CAMM2 vendor region registers (0x40 - 0x6F) are password protected registers. Both Read and Write access to CAMM2 vendor registers are blocked unless it is unlocked by providing the correct password. The default password for CAMM2 vendor register is 0x9473. The PMIC offers each CAMM2 vendors to select their own password for CAMM2 vendor registers.

### 8.2.2 Steps to Access CAMM2 Vendor Registers

The steps to access CAMM2 vendor registers are as follows:

1. Write to register [Table 159, Register 0x37](#) = 8 bit password LSB code
2. Write to register [Table 160, Register 0x38](#) = 8 bit password MSB code
3. Write to register [Table 161, Register 0x39](#) = 0x40.
4. Perform Read operations to CAMM2 vendor registers as desired.
5. Write to register [Table 161, Register 0x39](#) = 0x00.

### 8.2.3 Steps to Change CAMM2 Vendor Region Password

By default, the CAMM2 vendor region register password is 0x9473. The steps to change password from default password are as follows:

1. Write to register [Table 159, Register 0x37](#) = 0x73.
2. Write to register [Table 160, Register 0x38](#) = 0x94.
3. Write to register [Table 161, Register 0x39](#) = 0x40.
4. Write to register [Table 159, Register 0x37](#) = New 8 bit password LSB code as desired by CAMM2 vendor.
5. Write to register [Table 160, Register 0x38](#) = New 8 bit password MSB code as desired by CAMM2 vendor.
6. Write to register [Table 161, Register 0x39](#) = 0x80.
7. Wait 200 ms.
8. Write to register [Table 161, Register 0x39](#) = 0x00.
9. Power cycle the PMIC. (Remove VIN\_Bulk supply from the PMIC. The new password is in effect after the power cycle)

### 8.2.4 Steps to Burn or Program CAMM2 Vendor Region Registers

The steps to burn or to program CAMM2 vendor registers are as follows:

1. Write to register [Table 159, Register 0x37](#) = 8 bit password LSB code
2. Write to register [Table 160, Register 0x38](#) = 8 bit password MSB code
3. Write to register [Table 161, Register 0x39](#) = 0x40.
4. Programming CAMM2 vendor registers are done at block level. Block 40 addresses: 0x40 - 0x4F; Block 50 addresses: 0x50 - 0x5F; Block 60 addresses: 0x60 - 0x6F. Perform write operation to each block as desired.

## 8.2.4 Steps to Burn or Program CAMM2 Vendor Region Registers (cont'd)

5. Burn each block one at a time: Block 40 addresses: Write register [Table 161, Register 0x39](#) = 0x81. Block 50 addresses: Write register [Table 161, Register 0x39](#) = 0x82. Block 60 addresses: Write register [Table 161, Register 0x39](#) = 0x85. Note that there is an exception to Block 60 addresses. Four registers ([Table 211, Register 0x6D](#) [4,0], [Table 212, Register 0x6E](#) [4,0]) require different code which is [Table 161, Register 0x39](#) = 0x86.
6. Wait time 200 ms.
7. To check if programming is complete: Perform read from register [Table 161, Register 0x39](#). The code 0x5A indicates it is complete. It takes approximately 200 ms per page to program.
8. To verify if programming is done correctly: Perform read operation from appropriate block addresses.
9. Write to register [Table 161, Register 0x39](#) = 0x00.

## 8.3 Host Region Register Map

**Table 106 — Host Region - Register Map - Color Coding Scheme**

Region	Register Range	Restriction
Host Region + CAMM2 Vendor Region + Vendor Specific Region	<a href="#">Table 125, Register 0x15</a> to <a href="#">Table 151, Register 0x2F</a> , <a href="#">Table 154, Register 0x32</a> [7, 5:3,1:0], <a href="#">Table 157, Register 0x35</a> to <a href="#">Table 158, Register 0x36</a> [7:1], <a href="#">Table 166, Register 0x3E</a> , <a href="#">Table 167, Register 0x3F</a> [2], <a href="#">Table 182, Register 0x40</a> to Register 0x6F, Register 0x70 to Register 0xFF	Register Modification is NOT allowed in Secure Mode
Host Region	<a href="#">Table 132, Register 0x1C</a> to <a href="#">Table 149, Register 0x2D</a> , <a href="#">Table 150, Register 0x2E</a> [7:5, 3], <a href="#">Table 151, Register 0x2F</a> [2], <a href="#">Table 158, Register 0x36</a> [7:4], <a href="#">Table 166, Register 0x3E</a> [7:1]	Registers are copied from CAMM2 Vendor Region Setting at power on

**Table 107 — Host Region - Register Map**

Register	Attribute	Description
0x00 to 0x03	RV	R00 [7:0] to R03[7:0] - Reserved
<a href="#">Table 108, Register 0x04</a>	ROE	R04 [7] Global Error Count R04 [6] Global Error Log - Buck OV or UV R04 [5] Global Error Log - VIN_Bulk OV R04 [4] Global Error Log - Critical Temperature R04 [3:0] Reserved
<a href="#">Table 109, Register 0x05</a>	ROE	R05 [7] Reserved R05 [6:3] Power On Reset - SWA, SWD, SWB, SWC Power Not Good R05 [2:0] Power On Reset - High Level Error Log Code
<a href="#">Table 110, Register 0x06</a>	ROE	R06 [7:4] Power On Reset - SWA, SWD, SWB, SWC Under Voltage Lockout R06 [3:0] Power On Reset - SWA, SWD, SWB, SWC Over Voltage
<a href="#">Table 111, Register 0x07</a>	ROE	R07 [7:0] Reserved

**Table 107 — Host Region - Register Map (cont'd)**

Register	Attribute	Description
<a href="#">Table 112, Register 0x08</a>	RO	R08 [7] VIN_Bulk Input Power Good Status R08 [6] Critical Temperature Shutdown Status R08 [5:2] SWA, SWD, SWB, SWC Output Power Good Status R08 [1] Reserved R08 [0] VIN_Bulk Input Over Voltage Status
<a href="#">Table 113, Register 0x09</a>	RO	R09 [7] PMIC High Temperature Warning Status R09 [6] Reserved R09 [5] VOUT_1.8V Output Power Good Status R09 [4] Reserved R09 [3:0] SWA, SWD, SWB, SWC High Output Current Consumption Warning Status
<a href="#">Table 114, Register 0x0A</a>	RO	R0A [7:4] SWA, SWD, SWB, SWC Output Over Voltage Status R0A [3] PEC Error Status R0A [2] Parity Error Status R0A [1] IBI Status R0A [0] DVFSQ Power State Status
<a href="#">Table 115, Register 0x0B</a>	RO	R0B [7:4] SWA, SWD, SWB, SWC Output Current Limiter Warning Status R0B [3:0] SWA, SWD, SWB, SWC Output Under Voltage Lockout Status
<a href="#">Table 116, Register 0x0C</a>	RO	R0C [7:0] SWA Output Current or Power or Total Output Power Measurement
<a href="#">Table 117, Register 0x0D</a>	RO	R0D [7:0] SWD Output Current or Power Measurement
<a href="#">Table 118, Register 0x0E</a>	RO	R0E [7:0] SWB Output Current or Power Measurement
<a href="#">Table 119, Register 0x0F</a>	RO	R0F [7:0] SWC Output Current or Power Measurement
<a href="#">Table 120, Register 0x10</a>	1O	R10 [7] Clear VIN_Bulk Input Power Good Status R10 [6] Reserved R10 [5:2] Clear SWA, SWD, SWB, SWC Output Power Good Status R10 [1] Reserved R10 [0] Clear VIN_Bulk Input Over Voltage Status
<a href="#">Table 121, Register 0x11</a>	1O	R11 [7] Clear PMIC High Temperature Warning Status R11 [6] Reserved R11 [5] Clear VOUT_1.8V Output Power Good Status R11 [4] Reserved R11 [3:0] Clear SWA, SWD, SWB, SWC High Output Current Consumption Warning Status
<a href="#">Table 122, Register 0x12</a>	1O	R12 [7:4] Clear SWA, SWD, SWB, SWC Output Over Voltage Status R12 [3] Clear PEC Error R12 [2] Clear Parity Error R12 [1:0] Reserved
<a href="#">Table 123, Register 0x13</a>	1O	R13 [7:4] Clear SWA, SWD, SWB, SWC Output Current Limiter Warning Status R13 [3:0] Clear SWA, SWD, SWB, SWC Output Under Voltage Lockout Status
<a href="#">Table 124, Register 0x14</a>	1O	R14 [7:4] Reserved R14 [3] Clear VIN_Bulk Input Under Voltage Lockout Status R14 [2] Clear VOUT_1.0V Output Power Good Status R14 [1] Reserved R14 [0] Clear Global Status



**Table 107 — Host Region - Register Map (cont'd)**

Register	Attribute	Description
Table 125, Register 0x15	RW	R15 [7] Mask VIN_Bulk Input Power Good Status R15 [6] Reserved R15 [5:2] Mask SWA, SWD, SWB, SWC Output Power Good Status R15 [1] Reserved R15 [0] Mask VIN_Bulk Input Over Voltage Status
Table 126, Register 0x16	RW	R16 [7] Mask PMIC High Temperature Warning R16 [6] Reserved R16 [5] Mask VOUT_1.8V Output Power Good Status R16 [4] Reserved R16 [3:0] Mask SWA, SWD, SWB, SWC Output High Current Consumption Warning
Table 127, Register 0x17	RW	R17 [7:4] Mask SWA, SWD, SWB, SWC Output OV R17 [3] Mask PEC Error R17 [2] Mask Parity Error R17 [1:0] Reserved
Table 128, Register 0x18	RW	R18 [7:4] Mask SWA, SWD, SWB, SWC Output Current Limiter Warning R18 [3:0] Mask SWA, SWD, SWB, SWC Output UV Lockout
Table 129, Register 0x19	RW	R19 [7:4] Reserved R19 [3] Mask VIN_Bulk Input Under Voltage Lockout Status R19 [2] Mask VOUT_1.0 V Output Power Good Status R19 [1:0] Reserved
Table 130, Register 0x1A	RW	R1A [7:6] VIN_Bulk Power Good Threshold Voltage R1A [5] Reserved R1A [4] Quiescent Power State Entry Enable R1A [3] Reserved R1A [2] VOUT_1.8 V Power Good Threshold Voltage R1A [1] Output Power Select R1A [0] VOUT_1.0 V Power Good Threshold Voltage
Table 131, Register 0x1B	RW	R1B [7] VIN_Bulk Input Over Voltage Threshold R1B [6] Current or Power Meter Select R1B [5] Reserved R1B [4] Global Mask PWR_GOOD Output Pin R1B [3] Reserved R1B [2:0] PMIC High Temperature Warning Threshold
Table 132, Register 0x1C	RW	R1C [7:0] SWA Output High Current Threshold
Table 133, Register 0x1D	RW	R1D [7:0] SWD Output High Current Threshold
Table 134, Register 0x1E	RW	R1E [7:0] SWB Output High Current Threshold
Table 135, Register 0x1F	RW	R1F [7:0] SWC Output High Current Threshold
Table 136, Register 0x20	RW	R20 [7:6] SWA Output Current Limiter Warning Threshold R20 [5:4] SWD Output Current Limiter Warning Threshold R20 [3:2] SWB Output Current Limiter Warning Threshold R20 [1:0] SWC Output Current Limiter Warning Threshold
Table 137, Register 0x21	RW	R21 [7:1] SWA Voltage Setting R21 [0] SWA Power Good Low Side Threshold
Table 138, Register 0x22	RW	R22 [7:6] SWA Power Good High Side Threshold R22 [5:4] SWA Over Voltage Threshold R22 [3:2] SWA Under Voltage Lockout Threshold R22 [1:0] SWA Soft Stop Time

**Table 107 — Host Region - Register Map (cont'd)**

Register	Attribute	Description
Table 139, Register 0x23,	RW	R23 [7:1] SWD Voltage Setting
		R23 [0] SWD Power Good Low Side Threshold
Table 140, Register 0x24	RW	R24 [7:6] SWD Power Good High Side Threshold
		R24 [5:4] SWD Over Voltage Threshold
		R24 [3:2] SWD Under Voltage Lockout Threshold
		R24 [1:0] SWD Soft Stop Time
Table 141, Register 0x25,	RW	R25 [7:1] SWB Voltage Setting
		R25 [0] SWB Power Good Low Side Threshold
Table 142, Register 0x26,	RW	R26 [7:6] SWB Power Good High Side Threshold
		R26 [5:4] SWB Over Voltage Threshold
		R26 [3:2] SWB Under Voltage Lockout Threshold
		R26 [1:0] SWB Soft Stop Time
Table 143, Register 0x27,	RW	R27 [7:1] SWC Voltage Setting
		R27 [0] SWC Power Good Low Side Threshold
Table 144, Register 0x28,	RW	R28 [7:6] SWC Power Good High Side Threshold
		R28 [5:4] SWC Over Voltage Threshold
		R28 [3:2] SWC Under Voltage Lockout Threshold
		R28 [1:0] SWC Soft Stop Time
Table 145, Register 0x29,	RW	R29 [7:6] SWA Mode Select
		R29 [5:4] SWA Switching Frequency
		R29 [3:2] SWD Mode Select
		R29 [1:0] SWD Switching Frequency
Table 146, Register 0x2A,	RW	R2A [7:6] SWB Mode Select
		R2A [5:4] SWB Switching Frequency
		R2A [3:2] SWC Mode Select
		R2A [1:0] SWC Switching Frequency
Table 147, Register 0x2B,	RW	R2B [7:6] VOUT_1.8 V LDO Setting
		R2B [5:3] SWA, SWD, SWB Output Voltage Step Size
		R2B [2:1] VOUT_1.0 V LDO Setting
		R2B [0] SWC Output Voltage Step Size
Table 148, Register 0x2C,	RW	R2C [7:5] SWA Soft Start Time
		R2C [4] Reserved
		R2C [3:1] SWD Soft Start Time
		R2C [0] Reserved
Table 149, Register 0x2D,	RW	R2D [7:5] SWB Soft Start Time
		R2D [4] Reserved
		R2D [3:1] SWC Soft Start Time
		R2D [0] Reserved
Table 150, Register 0x2E	RW	R2E [7:6] SWB DVFSQ Voltage Slew Rate
	RW	R2E [5] SWB_Disable Input Pin Enable
	RW	R2E [4] DVFSQ_n Pin Enable
	RW	R2E [3] Unlock Pin Enable
	RW	R2E [2:0] PMIC Shutdown temperature threshold
Table 151, Register 0x2F	RW	R2F [7] Reserved
	RW	R2F [6:3] SWA, SWD, SWB, SWC Enable
	RW	R2F [2] Secure or Programmable Mode Select
	RW	R2F [1:0] Mask Bit Registers Control

**Table 107 — Host Region - Register Map (cont'd)**

Register	Attribute	Description
Table 152, Register 0x30	RW	R30 [7] ADC Enable R30 [6:3] ADC Select R30 [2] Register Addressing Mode R30 [1:0] ADC Register Update Frequency
Table 153, Register 0x31	RO	R31 [7:0] ADC Read Out
Table 154, Register 0x32	RW, RO	R32 [7] VR Enable R32 [6] Management Interface Selection R32 [5] PWR_GOOD Signal IO Type R32 [4:3] PMIC Power Good Output Signal Control R32 [2] Reserved R32 [1:0] ADC Accuracy Step Size
Table 155, Register 0x33	RO	R33 [7:5] Temperature Measurement R33 [4] Reserved R33 [3] VIN_Bulk Input Under Voltage Lockout Status R33 [2] VOUT_1.0V Output Power Good Status R33[1] DVFSQ_n Input Pin Level Status R33 [0] Unlock Input Pin Level Status
Table 156, Register 0x34	RO	R34 [7] PEC Enable R34 [6] IBI Enable R34 [5] Parity Disable R34 [4] Reserved R34 [3:1] HID_CODE R34 [0] Reserved
Table 157, Register 0x35	RW	R35 [7] Error Injection Enable R35 [6:4] Rail Selection R35 [3] Over and Under Voltage Select R35 [2:0] Misc. Error Injection Type
Table 158, Register 0x36	RW	R36 [7:4] Soft Stop Time Extension
	RW	R36 [3:1] Acoustic Noise Control
	RV	R36 [0] Reserved
Table 159, Register 0x37	WO	R37 [7:0] Password Lower Byte 0
Table 160, Register 0x38	WO	R38 [7:0] Password Upper Byte 1
Table 161, Register 0x39	RW	R39 [7:0] Command Codes
Table 162, Register 0x3A	RW	R3A [7] Reserved R3A [6] Default Read Address Pointer Enable R3A [5:4] Default Read Address Pointer Selection R3A [3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A [1:0] Reserved
Table 163, Register 0x3B	ROA	R3B [7:6] Reserved R3B [5:4] Major Revision ID R3B [3:1] Minor Revision ID R3B [0] PMIC Part ID
Table 164, Register 0x3C	ROA	R3C [7:0] VENDOR_ID_BYTE0
Table 165, Register 0x3D	ROA	R3D [7:0] VENDOR_ID_BYTE1
Table 166, Register 0x3E	RW	R3E [7:1] SWB DVFSQ Voltage Setting
	1O	R3E [0] Output Voltage Reset

**Table 107 — Host Region - Register Map (cont'd)**

Register	Attribute	Description
<a href="#">Table 167, Register 0x3F</a>	RW	R3F [7:3] Reserved R3F [2] SWB Voltage Offset R3F [1:0] Reserved
<a href="#">Table 168, Register 0x100</a>	RO	R100 [7:6] SWA Output Current or Power Measurement or Total Power Measurement MSB bits R100 [5:4] SWD Output Current or Power Measurement MSB bits R100 [3:2] SWB Output Current or Power Measurement MSB bits R100 [1:0] SWC Output Current or Power Measurement MSB bits
0x101	RV	R101 [7:0] Reserved
<a href="#">Table 169, Register 0x102</a>	RO	R102 [7:0] SWA Output Current or Power Measurement or Total Power Measurement LSB bits
<a href="#">Table 170, Register 0x103</a>	RO	R103 [7:0] SWD Output Current or Power Measurement LSB bits
<a href="#">Table 171, Register 0x104</a>	RO	R104 [7:0] SWB Output Current or Power Measurement LSB bits
<a href="#">Table 172, Register 0x105</a>	RO	R105 [7:0] SWC Output Current or Power Measurement LSB bits
0x106 - 0x108	RV	R106 [7:0] to R108 [7:0] Reserved
<a href="#">Table 173, Register 0x109</a>	RO	R109 [7:1] Reserved R109 [0] SWB_Disable Input Pin Level Status at VR_EN Command
0x10A - 0x12F	RV	R10A [7:0] to R12F [7:0] Reserved
<a href="#">Table 174, Register 0x130</a>	ROA	R130 [7:0] Serial Number - Byte 0
<a href="#">Table 175, Register 0x131</a>	ROA	R131 [7:0] Serial Number - Byte 1
<a href="#">Table 176, Register 0x132</a>	ROA	R132 [7:0] Serial Number - Byte 2
<a href="#">Table 177, Register 0x133</a>	ROA	R133 [7:0] Serial Number - Byte 3
<a href="#">Table 178, Register 0x134</a>	ROA	R134 [7:0] Serial Number - Byte 4
<a href="#">Table 179, Register 0x135</a>	ROA	R135 [7:0] Serial Number - Byte 5
<a href="#">Table 180, Register 0x136</a>	ROA	R136 [7:0] Serial Number - Byte 6
0x137 - 0x13F	RV	R135 [7:0] to R13F [7:0] Reserved

## 8.4 Register Definition

### 8.4.1 Status Registers

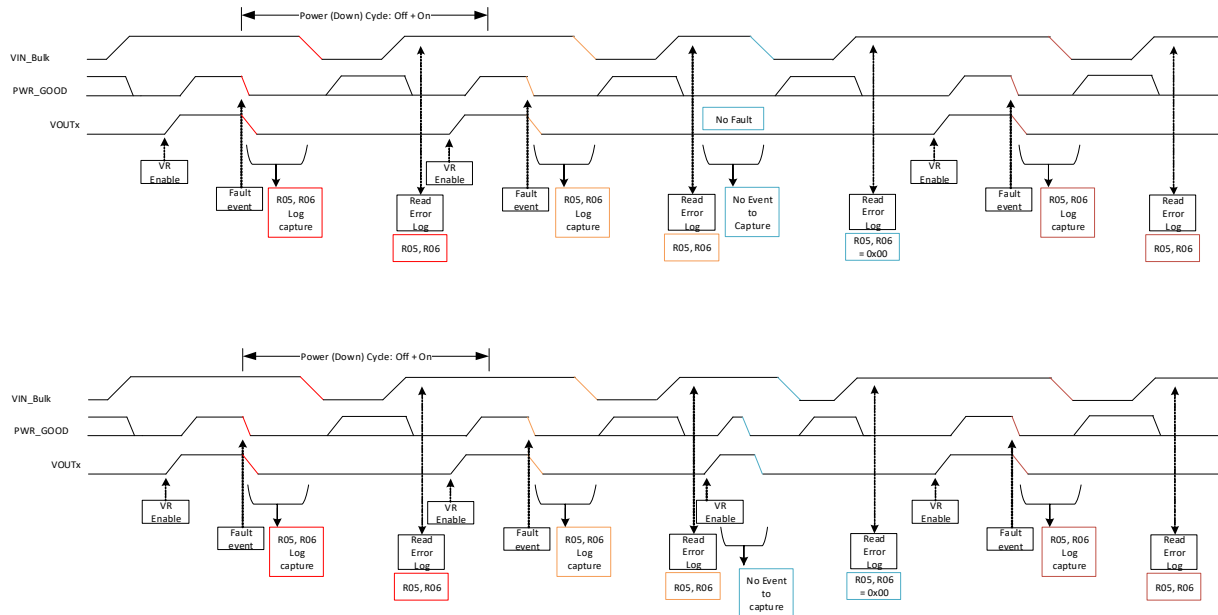
The DDR5 PMIC offers status registers that are grouped into four different categories.

1. Global History of Error Log Register ([Table 108, Register 0x04 \[7:4\]](#))
2. Error Log Registers ([Table 109, Register 0x05 \[6:0\]](#), [Table 110, Register 0x06 \[7:0\]](#), [Table 111, Register 0x07 \[7:0\]](#); [Table 111, Register 0x07 \[7:0\]](#) is currently defined as Reserved)
3. Real time Status Registers ([Table 112, Register 0x08 \[6:2,0\]](#), [Table 113, Register 0x09 \[7,5,3:0\]](#), [Table 114, Register 0x0A \[7:0\]](#), [Table 115, Register 0x0B \[7:0\]](#), [Table 155, Register 0x33 \[4:2\]](#), [Table 173, Register 0x109 \[0\]](#))
4. Periodic Status Registers ([Table 116, Register 0x0C](#), [Table 117, Register 0x0D](#), [Table 118, Register 0x0E](#), [Table 119, Register 0x0F](#), [Table 155, Register 0x33 \[7:5\]](#), [Table 168, Register 0x100](#), [Table 169, Register 0x102](#), [Table 170, Register 0x103](#), [Table 171, Register 0x104](#), [Table 172, Register 0x105](#))

Global History of Error Log Register ([Table 108, Register 0x04 \[7:4\]](#)) - This register records the PMIC state at each abnormal power down cycle. This register reports the cumulative error of each abnormal power down sequence. The PMIC writes this register on its own when it internally generates VR Disable command on its own due to failure. The host can erase this register in MTP memory and clear the status register by writing the code 0x74 in [Table 161, Register 0x39](#).

- Error Log Registers ([Table 109, Register 0x05 \[6:0\]](#), [Table 110, Register 0x06 \[7:0\]](#), [Table 111, Register 0x07 \[7:0\]](#)) - These registers record the PMIC state at each power down sequence. The PMIC may report an abnormal power down sequence or a normal power down sequence. The PMIC writes these registers and updates MTP when it internally generates a VR Disable command on its own due to failure. At the next power up, the registers are restored from MTP to be read by the host, and MTP is cleared by the PMIC. A value of '0' in the register indicates no fault event occurred prior to previous power down cycle.
- The host can clear the status registers and MTP by writing the code 0x74 in [Table 161, Register 0x39](#).
- See [Figure 43](#) for illustration. The top waveform illustrates how PMIC captures Error Log Registers ([Table 109, Register 0x05](#) to [Table 111, Register 0x07](#)) when there is a fault and how PMIC reports error log registers when PMIC goes through power cycle. The bottom waveform illustrates same as top waveform with one exception. It shows no fault condition when PWR\_GOOD is asserted to turn off switch regulator outputs with power down sequence. The phrase "Power Cycle" is used interchangeably with "Power Down Cycle" as illustrated in both figures and it means VIN\_Bulk input supply is removed and re-applied. "Power Down Sequence" means execution of Power Off Sequence configuration registers ([Table 200, Register 0x58](#) to [Table 203, Register 0x5B](#)).

## 8.4.1 Status Registers (cont'd)



**Figure 43 — Error Log (R05 to R07) Registers Behavior with Power Cycle**

Real Time Status Registers ([Table 112, Register 0x08 \[6:2,0\]](#), [Table 113, Register 0x09 \[7,5,3:0\]](#), [Table 114, Register 0x0A \[7:1\]](#), [Table 115, Register 0x0B \[7:0\]](#), [Table 155, Register 0x33 \[2\]](#)) - These registers are updated to '1' any time based on any event that occurs. The status registers will remain at '1' even if the failing condition is no longer present until the Clear Register command is received by the PMIC. Note that any switch regulator related status registers are only applicable after VR Enable command is registered by the PMIC. The PMIC updates switch regulators related status registers after VR Enable command is registered within tPMIC\_PWR\_GOOD\_OUT time if there is any issue and host shall check these status registers if there is any event related to switch regulators in future. The PWR\_GOOD interrupt may be generated by the PMIC at the same time depending on the type of event. The interrupts are only generated if they are not masked. The status registers [Table 112, Register 0x08 \[7\]](#), [Table 113, Register 0x09 \[5\]](#), and [Table 155, Register 0x33 \[2\]](#) is only valid once valid VIN\_Bulk input supply is valid at the PMIC input pin. The remaining status registers are valid after VR Enable command is registered.

Periodic Status Registers ([Table 116, Register 0x0C](#), [Table 117, Register 0x0D](#), [Table 118, Register 0x0E](#), [Table 119, Register 0x0F](#), [Table 155, Register 0x33 \[7:5\]](#)) - These registers are updated periodically. These registers are only valid after VR Enable command is registered.

All Read Only (RO) registers except for registers [Table 116, Register 0x0C](#), [Table 117, Register 0x0D](#), [Table 118, Register 0x0E](#), [Table 119, Register 0x0F](#), and [Table 155, Register 0x33 \[7:5\]](#) are one time latched registers. In other words, once PMIC sets those register flag, the host must explicitly clear those registers appropriately. The PMIC does not automatically update the registers on its own even if the event that triggered the status is no longer present. The registers [Table 116, Register 0x0C](#), [Table 117, Register 0x0D](#), [Table 118, Register 0x0E](#), [Table 119, Register 0x0F](#), and [Table 155, Register 0x33](#) are dynamically updated by the PMIC at certain frequency and they represent the status at that point.

## 8.4.1 Status Registers (cont'd)

**Table 108 — Register 0x04**

R04			
Bits	Attribute	Default	Description <sup>[1],[2],[3]</sup>
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation <sup>[4]</sup> 0 = No Error or Only 1 Error since last Erase operation 1 = > 1 Error Count since last Erase operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Over or Under Voltage <sup>[5]</sup> 0 = No Error Occurred 1 = Error Occurred
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOLTAGE Global Error Log History for VIN_Bulk Over Voltage <sup>4</sup> 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature <sup>4</sup> 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	R04 [3:0]: Reserved

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs a minimum of 3.0 V for VIN\_Bulk voltage and 200 ms duration from PWR\_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 Host must explicitly perform Erase operation to erase this entire register via command in [Table 161, Register 0x39](#). The PMIC needs minimum of 200 ms for Erase operation.

NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation.

NOTE 4 PMIC counts the error since last erase operation and if more than one error occurs, it sets this bit to '1'. Host must explicitly perform Erase operation to erase this entire register [Table 108, Register 0x04 \[7:0\]](#).

NOTE 5 PMIC sets the bit when error occurs.

## 8.4.1 Status Registers (cont'd)

Table 109 — Register 0x05

R05			
Bits	Attribute	Default	Description <sup>[1],[2],[3]</sup>
7	ROE	0	R0 5 [7]: Reserved
6	ROE	0	R05 [6]: SWA_POWER_GOOD PMIC Power On - SWA Power Not Good <sup>[4]</sup> 0 = Normal Power On 1 = Power On - SWA Power Not Good
5	ROE	0	R05 [5]: PMIC Power On - SWD Power Not Good <sup>3</sup> 0 = Normal Power On 1 = Power On - SWD Power Not Good
4	ROE	0	R05 [4]: SWB_POWER_GOOD PMIC Power On - SWB Power Not Good <sup>3</sup> 0 = Normal Power On 1 = Power On - SWB Power Not Good
3	ROE	0	R05 [3]: SWC_POWER_GOOD PMIC Power On - SWC Power Not Good <sup>3</sup> 0 = Normal Power On 1 = Power On - SWC Power Not Good
2:0	ROE	0	R05 [2:0]: PMIC_ERROR_LOG PMIC Power On - High Level Status Bit to Indicate Last Known Power Cycle or System Reset 000 = Normal Power On 001 = Reserved 010 = Buck Regulator Output Over or Under Voltage <sup>[5]</sup> 011 = Critical Temperature 100 = VIN_Bulk Input Over Voltage 101 = Reserved 110 = Reserved 111 = VIN_Bulk Input Under Voltage

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 3.0 V for VIN\_Bulk voltage and 200 ms duration from PWR\_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via [Table 161, Register 0x39](#). The PMIC needs a minimum of 200 ms for Erase operation.

NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation.

NOTE 4 This register is set only if PMIC generates internal VR Disable command due to fault condition.

NOTE 5 This code is a logical OR function of [Table 110, Register 0x06](#) [7:0] register bits.



## 8.4.1 Status Registers (cont'd)

**Table 110 — Register 0x06**

Bits	R06		
	Attribute	Default	Description <sup>[1],[2],[3]</sup>
7	ROE	0	R06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWA Under Voltage Lockout 0 = Normal Power On 1 = Power On - SWA Under Voltage Lockout
6	ROE	0	R06 [6]: SWD_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWD Under Voltage Lockout 0 = Normal Power On 1 = Power On - SWD Under Voltage Lockout
5	ROE	0	R06 [5]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWB Under Voltage Lockout 0 = Normal Power On 1 = Power On - SWB Under Voltage Lockout
4	ROE	0	R06 [4]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power On - SWC Under Voltage Lockout 0 = Normal Power On 1 = Power On - SWC Under Voltage Lockout
3	ROE	0	R06 [3]: SWA_OVER_VOLTAGE PMIC Power On - SWA Over Voltage 0 = Normal Power On 1 = Power On - SWA Over Voltage
2	ROE	0	R06 [2]: SWD_OVER_VOLTAGE PMIC Power On - SWD Over Voltage 0 = Normal Power On 1 = Power On - SWD Over Voltage
1	ROE	0	R06 [1]: SWB_OVER_VOLTAGE PMIC Power On - SWB Over Voltage 0 = Normal Power On 1 = Power On - SWB Over Voltage
0	ROE	0	R06 [0]: SWC_OVER_VOLTAGE PMIC Power On - SWC Over Voltage 0 = Normal Power On 1 = Power On - SWC Over Voltage

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 3.0 V for VIN\_Bulk voltage and 200 ms duration from PWR\_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via [Table 161, Register 0x39](#). The PMIC needs a minimum of 200 ms for Erase operation.

NOTE 3 The error log registers are only updated when there is a VR Disable fault when the buck regulators are under regulation.

### 8.4.1 Status Registers (cont'd)

**Table 111 — Register 0x07**

R07			
Bits	Attribute	Default	Description <sup>[1],[2]</sup>
7:0	ROE	0	R07 [7:0]: Reserved

NOTE 1 The PMIC always attempts to write this register into its non-volatile memory. However, it may not be guaranteed depending on how fast the host may shut off the input power to the PMIC. The PMIC needs minimum of 3.0 V for VIN\_Bulk voltage and 200 ms duration from PWR\_GOOD signal assertion to guarantee the write operation into non-volatile memory.

NOTE 2 This entire register status reflects previous power down cycle of the PMIC and is updated by the PMIC on its own at each power cycle, if update is needed. Because this register is updated only if there is an update needed, there is no NVM life time impact. This register is cleared when host issues the erase command via [Table 161, Register 0x39](#). The PMIC needs a minimum of 200 ms for Erase operation.

## 8.4.1 Status Registers (cont'd)

**Table 112 — Register 0x08**

R08			
Bits	Attribute	Default	Description
7	RO	0	R08 [7]: VIN_BULK_INPUT_POWER_GOOD_STATUS VIN_Bulk Input Power Good Status <sup>[1]</sup> 0 = Power Good 1 = Power Not Good
6	RO	0	R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status <sup>[2]</sup> 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	R08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status <sup>[3]</sup> 0 = Power Good 1 = Power Not Good
4	RO	0	R08 [4]: SWD_OUTPUT_POWER_GOOD_STATUS Switch Node D Output Power Good Status <sup>[4]</sup> 0 = Power Good 1 = Power Not Good
3	RO	0	R08 [3]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status <sup>[5]</sup> 0 = Power Good 1 = Power Not Good
2	RO	0	R08 [2]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status <sup>[6]</sup> 0 = Power Good 1 = Power Not Good
1	RV	0	R08 [1]: Reserved
0	RO	0	R08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_Bulk Input Supply Over Voltage Status <sup>[7]</sup> 0 = No Over Voltage 1 = Over Voltage

NOTE 1 This register is set when VIN\_Bulk input goes below the threshold setting in register [Table 130, Register 0x1A](#) [7:6].

NOTE 2 This register is set when PMIC temperature goes above the threshold setting in register [Table 150, Register 0x2E](#) [2:0].

NOTE 3 This register is set when SWA output voltage goes either below the threshold setting in register [Table 137, Register 0x21](#), [0] or above the threshold setting in register [Table 138, Register 0x22](#), [7:6].

NOTE 4 This register is set when SWD output goes either below the threshold setting in register [Table 139, Register 0x23](#), [0] or above the threshold setting in register [Table 140, Register 0x24](#) [7:6].

NOTE 5 This register is set when SWB output goes either below the threshold setting in register [Table 141, Register 0x25](#), [0] or above the threshold setting in register [Table 142, Register 0x26](#), [7:6].

NOTE 6 This register is set when SWC output goes either below the threshold setting in register [Table 143, Register 0x27](#), [0] or above the threshold setting in register [Table 144, Register 0x28](#), [7:6].

NOTE 7 This register is set when VIN\_Bulk input voltage goes above the threshold setting in register [Table 131, Register 0x1B](#) [7].

## 8.4.1 Status Registers (cont'd)

Table 113 — Register 0x09

R09			
Bits	Attribute	Default	Description
7	RO	0	R09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status <sup>[1]</sup> 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RV	0	R09 [6]: Reserved
5	RO	0	R09 [5]: VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS VOUT_1.8V LDO Output Power Good Status <sup>[2]</sup> 0 = Power Good 1 = Power Not Good
4	RV	0	R09 [4]: Reserved
3	RO	0	R09 [3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node A High Output Current Consumption Warning Status <sup>[3]</sup> 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
2	RO	0	R09 [2]: SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node D High Output Current Consumption Warning Status <sup>[4]</sup> 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
1	RO	0	R09 [1]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node B High Output Current Consumption Warning Status <sup>[5]</sup> 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
0	RO	0	R09 [0]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Switch Node C High Output Current Consumption Warning Status <sup>[6]</sup> 0 = No High Current Consumption Warning 1 = High Current Consumption Warning

NOTE 1 This register is set when PMIC temperature goes above the threshold setting in [Table 131, Register 0x1B \[2:0\]](#).

NOTE 2 This register is set when VOUT\_1.8V output exceeds the threshold setting in register [Table 130, Register 0x1A \[2\]](#).

NOTE 3 This register is set when SWA output current consumption goes above the threshold setting in [Table 132, Register 0x1C \[7:0\]](#).

NOTE 4 This register is set when SWD output current consumption goes above the threshold setting in [Table 133, Register 0x1D \[7:0\]](#).

NOTE 5 This register is set when SWB output current consumption goes above the threshold setting in [Table 134, Register 0x1E \[7:0\]](#).

NOTE 6 This register is set when SWC output current consumption goes above the threshold setting in [Table 135, Register 0x1F \[7:0\]](#).

## 8.4.1 Status Registers (cont'd)

**Table 114 — Register 0x0A**

R0A			
Bits	Attribute	Default	Description
7	RO	0	R0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Over Voltage Status <sup>[1]</sup> 0 = No Over Voltage 1 = Over Voltage
6	RO	0	R0A [6]: SWD_OUTPUT_OVER_VOLTAGE_STATUS Switch Node D Output Over Voltage Status <sup>[2]</sup> 0 = No Over Voltage 1 = Over Voltage
5	RO	0	R0A [5]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Over Voltage Status <sup>[3]</sup> 0 = No Over Voltage 1 = Over Voltage
4	RO	0	R0A [4]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Over Voltage Status <sup>[4]</sup> 0 = No Over Voltage 1 = Over Voltage
3	RO	0	R0A [3]: PEC_ERROR_STATUS Packet Error Code Status <sup>[5],[6]</sup> 0 = No PEC Error 1 = PEC Error
2	RO	0	R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status <sup>6,[7]</sup> 0 = No Parity Error 1 = Parity Error
1	RO	0	R0A [1]: IBI_AND_GLOBAL_STATUS In Band Interrupt and Global Status <sup>[8]</sup> 0 = No Pending IBI or Outstanding Status 1 = Pending IBI or Outstanding Status
0	RO	0	R0A [0]: DVFSQ_POWER_STATE_STATUS PMIC DVFSQ Power State Status <sup>[9],[10],[11]</sup> 0 = PMIC is not operating in the DVFSQ Power State 1 = PMIC is operating in the DVFSQ Power State

NOTE 1 This register is set when SWA output voltage goes above the threshold setting in [Table 138, Register 0x22](#), [5:4].

NOTE 2 This register is set when SWD output voltage goes above the threshold setting in [Table 140, Register 0x24](#) [5:4]

NOTE 3 This register is set when SWB output voltage goes above the threshold setting in [Table 142, Register 0x26](#), [5:4]

NOTE 4 This register is set when SWC output voltage goes above the threshold setting in [Table 144, Register 0x28](#), [5:4]

NOTE 5 Applicable in I3C Mode Only and if enabled in register [Table 156, Register 0x34](#) [7].

NOTE 6 This register is updated when PMIC device goes through bus reset as described in clause 5.4.13.

NOTE 7 Applicable in I3C Mode and if enabled in register [Table 156, Register 0x34](#) [5]. It is also applicable in I<sup>2</sup>C mode for supported CCCs.

NOTE 8 This register can be used as Global Status in addition to IBI status. When IBI function is enabled, this register is automatically cleared when PMIC transmits IBI payload; however, individual status registers still require an explicit clear command from host.

NOTE 9 If [Table 150, Register 0x2E](#) [4] = '1', this register is set when PMIC detects DVFSQ\_n input transitions from high to low and is cleared when PMIC detects DVFSQ\_n input transitions from low to high. The PMIC also clears this register when VR Disable command is registered (either with VR\_EN pin de-assertion or via I<sup>2</sup>C/I3C bus command).

NOTE 10 The controller cannot clear this register via any I<sup>2</sup>C/I3C bus command.

NOTE 11 This status register is not applicable and it is a don't care when [Table 150, Register 0x2E](#) [5] = '1'.

## 8.4.1 Status Registers (cont'd)

**Table 115 — Register 0x0B**

R0B			
Bits	Attribute	Default	Description
7	RO	0	R0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status <sup>[1]</sup> 0 = No Current Limiter Event 1 = Current Limiter Event
6	RO	0	R0B [6]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node D Output Current Limiter Warning Status <sup>[2]</sup> 0 = No Current Limiter Event 1 = Current Limiter Event
5	RO	0	R0B [5]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status <sup>[3]</sup> 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	R0B [4]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status <sup>[4]</sup> 0 = No Current Limiter Event 1 = Current Limiter Event
3	RO	0	R0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Under Voltage Lockout Status <sup>[5]</sup> 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
2	RO	0	R0B [2]: SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node D Output Under Voltage Lockout Status <sup>[6]</sup> 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
1	RO	0	R0B [1]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Under Voltage Lockout Status <sup>[7]</sup> 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
0	RO	0	R0B [0]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Under Voltage Lockout Status <sup>[8]</sup> 0 = No Under Voltage Lockout 1 = Under Voltage Lockout

NOTE 1 This register is set when SWA output valley current goes above the threshold setting in [Table 136, Register 0x20](#) [7:6].

NOTE 2 This register is set when SWC output valley current goes above the threshold setting in [Table 136, Register 0x20](#) [5:4].

NOTE 3 This register is set when SWB output valley current goes above the threshold setting in [Table 136, Register 0x20](#) [3:2].

NOTE 4 This register is set when SWC output valley current goes above the threshold setting in [Table 136, Register 0x20](#) [1:0].

NOTE 5 This register is set when SWA output voltage goes below the threshold setting in [Table 138, Register 0x22](#), [3:2].

NOTE 6 This register is set when SWC output voltage goes below the threshold setting in [Table 140, Register 0x24](#) [3:2].

NOTE 7 This register is set when SWB output voltage goes below the threshold setting in [Table 142, Register 0x26](#), [3:2].

NOTE 8 This register is set when SWC output voltage goes below the threshold setting in [Table 144, Register 0x28](#), [3:2].

## 8.4.1 Status Registers (cont'd)

**Table 116 — Register 0x0C**

R0C			
Bits	Attribute	Default	Description <sup>[1]</sup>
7:0	RO		<p>R0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node A Output Current or Output Power<sup>[2]</sup> Measurement<sup>[3]</sup></p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '0':            0000 0000 = Undefined            0000 0001 = 125 mA or 125 mW            0000 0010 = 250 mA or 250 mW            0000 0011 = 375 mA or 375 mW            0000 0100 = 500 mA or 500 mW            ...            1111 1111 <math>\geq</math> 31.875A or 31.875 W</p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '1':            Sum of SWA, SWD, SWB and SWC Output Power<sup>[4]</sup>            0000 0000 = Undefined            0000 0001 = 125 mW            0000 0010 = 250 mW            0000 0011 = 375 mW            0000 0100 = 500 mW            ...            1111 1111 <math>\geq</math> 31.875 W</p>

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 3 This register is only applicable if [Table 154, Register 0x32](#) [1:0] = '00'.

NOTE 4 Register [Table 131, Register 0x1B](#) [6] must be configured as '1'.

## 8.4.1 Status Registers (cont'd)

Table 117 — Register 0x0D

R0D			
Bits	Attribute	Default	Description <sup>[1]</sup>
7:0	RO		R0D [7:0]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node D Output Current or Output Power <sup>[2]</sup> Measurement <sup>[3]</sup>  If <a href="#">Table 130, Register 0x1A</a> [1] = '0': 0000 0000 = Undefined 0000 0001 = 125 mA or 125 mW 0000 0010 = 250 mA or 250 mW 0000 0011 = 375 mA or 375 mW 0000 0100 = 500 mA or 500 mW ... 0011 1111 $\geq$ 7.875A or 7.875 W

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 3 This register is only applicable if [Table 154, Register 0x32](#) [1:0] = '00'.

Table 118 — Register 0x0E

R0E			
Bits	Attribute	Default	Description <sup>[1]</sup>
7:0	RO		R0E [7:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power <sup>[2]</sup> Measurement <sup>[3]</sup>  If <a href="#">Table 130, Register 0x1A</a> [1] = '0': 0000 0000 = Undefined 0000 0001 = 125 mA or 125 mW 0000 0010 = 250 mA or 250 mW 0000 0011 = 375 mA or 375 mW 0000 0100 = 500 mA or 500 mW ... 0011 1111 $\geq$ 7.875A or 7.875 W

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 3 This register is only applicable if [Table 154, Register 0x32](#) [1:0] = '00'.



### 8.4.1 Status Registers (cont'd)

**Table 119 — Register 0x0F**

R0F			
Bits	Attribute	Default	Description <sup>[1]</sup>
7:0	RO		<p>R0F [7:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power<sup>[2]</sup> Measurement<sup>[3]</sup></p> <p>If <a href="#">Table 130, Register 0x1A</a> [1] = '0'</p> <p>0000 0000 = Undefined  0000 0001 = 125 mA or 125 mW  0000 0010 = 250 mA or 250 mW  0000 0011 = 375 mA or 375 mW  0000 0100 = 500 mA or 500 mW  ...  xx11 1111 <math>\geq</math> 7.875A or 7.875 W</p>

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 3 This register is only applicable if [Table 154, Register 0x32](#) [1:0] = '00'.

## 8.4.2 Clear Registers

For each Real Time Status Registers ([Table 112, Register 0x08 \[6:2,0\]](#), [Table 113, Register 0x09 \[7,5,3:0\]](#), [Table 114, Register 0x0A \[7:1\]](#), [Table 115, Register 0x0B \[7:0\]](#), and [Table 155, Register 0x33 \[3:2\]](#)), the CAMM2 PMIC offers a way to clear the status of each event. The clear registers are [Table 120, Register 0x10 \[5:2,0\]](#), [Table 121, Register 0x11 \[7,5,3:0\]](#), [Table 122, Register 0x12 \[7:2\]](#), [Table 123, Register 0x13 \[7:0\]](#), and [Table 124, Register 0x14 \[3:2\]](#), respectively. All clear registers are write '1' only registers. When '1' is written to any of the clear registers, the PMIC updates the status registers to default state and removes the interrupt condition on GSI\_n and PWR\_GOOD output signal, assuming that event is no longer present. If the failing condition is still present, the status register will still remain at '1'. Note that GSI\_n and PWR\_GOOD interrupt is only applicable if that event is not masked. GSI\_n output signal can be disabled.

When '1' is written to any of the clear registers, there are three categories of response by the PMIC.

- PMIC removes GSI\_n interrupt (PWR\_GOOD interrupt is not applicable). Related status registers are: [Table 121, Register 0x11 \[7,3:0\]](#), [Table 122, Register 0x12 \[3:2\]](#), [Table 123, Register 0x13 \[7:4\]](#).
- PMIC removes GSI\_n and PWR\_GOOD interrupt. Related status registers are: [Table 120, Register 0x10 \[5:2\]](#), [Table 121, Register 0x11 \[5\]](#), [Table 124, Register 0x14 \[2\]](#).
- PMIC only removes GSI\_n interrupt and does not remove PWR\_GOOD interrupt. Related status registers are: [Table 120, Register 0x10 \[0\]](#), [Table 122, Register 0x12 \[7:4\]](#), [Table 123, Register 0x13 \[3:0\]](#), [Table 124, Register 0x14 \[3\]](#). The host is expected to either power cycle the PMIC or re-issue the VR Enable command if PMIC is in programmable mode.

Note that PMIC does not allow controller to clear these status registers via I<sup>2</sup>C/I<sup>3</sup>C bus command: [Table 114, Register 0x0A \[0\]](#), [Table 155, Register 0x33 \[1:0\]](#) and [Table 173, Register 0x109 \[0\]](#).

The PMIC offers a Global Clear command by writing '1' to registers [Table 124, Register 0x14 \[0\]](#). This command works same way as individual clear command. This command can alternatively be used by the host if more than one clear command is required for different registers.

**Table 120 — Register 0x10**

R10			
Bits	Attribute	Default	Description <sup>[1]</sup>
7	1O	0	R10 [7]: CLEAR_VIN_BULK_INPUT_POWER_GOOD_STATUS Clear VIN_Bulk Input Power Good Status 1 = Clear Register <a href="#">Table 112, Register 0x08 [7]</a> <sup>[2]</sup>
6	RV	0	R10 [6]: Reserved
5	1O	0	R10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear Register <a href="#">Table 112, Register 0x08 [5]</a> <sup>[2]</sup>
4	1O	0	R10 [4]: CLEAR_SWD_OUTPUT_POWER_GOOD_STATUS Clear SWD Output Power Good Status. 1 = Clear Register <a href="#">Table 112, Register 0x08 [4]</a> <sup>[2]</sup>
3	1O	0	R10 [3]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS Clear SWB Output Power Good Status. 1 = Clear Register <a href="#">Table 112, Register 0x08 [3]</a> <sup>[2]</sup>
2	1O	0	R10 [2]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear Register <a href="#">Table 112, Register 0x08 [2]</a> <sup>[2]</sup>
1	RV	0	R10 [1]: Reserved
0	1O	0	R10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear VIN_Bulk Input Supply Over Voltage Status. 1 = Clear Register <a href="#">Table 112, Register 0x08 [0]</a> <sup>[2]</sup>

NOTE 1 [Table 120, Register 0x10 \[5:2,0\]](#) are self clearing bits.

NOTE 2 See [Table 28](#) and [Table 29](#) for POWER\_GOOD output signal status change.

## 8.4.1 Status Registers (cont'd)

Table 121 — Register 0x11

R11			
Bits	Attribute	Default	Description <sup>[1]</sup>
7	10	0	R11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status. 1 = Clear Register <a href="#">Table 113, Register 0x09</a> [7] <sup>[2]</sup>
6	RV	0	R11 [6]: Reserved
5	10	0	R11 [5]: CLEAR_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.8V Output Power Good Status. 1 = Clear Register <a href="#">Table 113, Register 0x09</a> [5] <sup>[2]</sup>
4	RV	0	R11 [4]: Reserved
3	10	0	R11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear Register <a href="#">Table 113, Register 0x09</a> [3] <sup>[2]</sup>
2	10	0	R11 [2]: CLEAR_SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node D High Output Current Consumption Warning Status. 1 = Clear Register <a href="#">Table 113, Register 0x09</a> [2] <sup>[2]</sup>
1	10	0	R11 [1]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status. 1 = Clear Register <a href="#">Table 113, Register 0x09</a> [1] <sup>[2]</sup>
0	10	0	R11 [0]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. 1 = Clear Register <a href="#">Table 113, Register 0x09</a> [0] <sup>[2]</sup>

NOTE 1 [Table 121, Register 0x11](#) [7,5,3:0] are self clearing bits.NOTE 2 See [Table 28](#) and [Table 29](#) for POWER\_GOOD output signal status change.

Table 122 — Register 0x12

R12			
Bits	Attribute	Default	Description <sup>[1]</sup>
7	10	0	R12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Over Voltage Status. 1 = Clear Register <a href="#">Table 114, Register 0x0A</a> [7] <sup>[2]</sup>
6	10	0	R12 [6]: CLEAR_SWD_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node D Output Over Voltage Status. 1 = Clear Register <a href="#">Table 114, Register 0x0A</a> [6] <sup>[2]</sup>
5	10	0	R12 [5]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node B Output Over Voltage Status. 1 = Clear Register <a href="#">Table 114, Register 0x0A</a> [5] <sup>[2]</sup>
4	10	0	R12 [4]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Over Voltage Status. 1 = Clear Register <a href="#">Table 114, Register 0x0A</a> [4] <sup>[2]</sup>
3	10	0	R12 [3]: CLEAR_PEC_ERROR_STATUS Clear PEC Error Status. 1 = Clear Register <a href="#">Table 114, Register 0x0A</a> [3]
2	10	0	R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear Register <a href="#">Table 114, Register 0x0A</a> [2]
1:0	RV	0	R12 [1:0]: Reserved

NOTE 1 [Table 122, Register 0x12](#) [7:1] are self clearing bits.NOTE 2 See [Table 28](#) and [Table 29](#) for POWER\_GOOD output signal status change.

## 8.4.1 Status Registers (cont'd)

Table 123 — Register 0x13

R13			
Bits	Attribute	Default	Description <sup>[1]</sup>
7	1O	0	R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [7] <sup>[2]</sup>
6	1O	0	R13 [6]: CLEAR_SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node D Output Current Limiter Warning Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [6] <sup>[2]</sup>
5	1O	0	R13 [5]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [5] <sup>[2]</sup>
4	1O	0	R13 [4]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [4] <sup>[2]</sup>
3	1O	0	R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Under Voltage Lockout Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [3] <sup>[2]</sup>
2	1O	0	R13 [2]: CLEAR_SWD_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node D Output Under Voltage Lockout Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [2] <sup>[2]</sup>
1	1O	0	R13 [1]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Under Voltage Lockout Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [1] <sup>[2]</sup>
0	1O	0	R13 [0]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Under Voltage Lockout Status. 1 = Clear Register <a href="#">Table 115, Register 0x0B</a> [0] <sup>[2]</sup>

NOTE 1 [Table 123, Register 0x13](#) [7:0] are self clearing bits.NOTE 2 See [Table 28](#) and [Table 29](#) for POWER\_GOOD output signal status change.

Table 124 — Register 0x14

R14			
Bits	Attribute	Default	Description <sup>[1]</sup>
7:4	RV	0	R14 [7:4]: Reserved
3	1O	0	R14 [3]: CLEAR_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Clear VIN_Bulk Input Under Voltage Lockout Status 1 = Clear Register <a href="#">Table 155, Register 0x33</a> [3]
2	1O	0	R14 [2]: CLEAR_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.0V Output Power Good Status. 1 = Clear Register <a href="#">Table 155, Register 0x33</a> [2] <sup>[3]</sup>
1	RV	0	R14 [1]: Reserved
0	1O	0	R14 [0]: GLOBAL_CLEAR_STATUS Clear all <sup>[2]</sup> status bits. 1 = Clear all status bits <sup>[3]</sup>

NOTE 1 [Table 124, Register 0x14](#) [3:2,0] are self clearing bits.NOTE 2 All status bits in register [Table 120, Register 0x10](#) [5:2,0], [Table 121, Register 0x11](#) [7,5,3:0], [Table 122, Register 0x12](#) [7:2], [Table 123, Register 0x13](#) [7:0], and [Table 124, Register 0x14](#) [3:2].NOTE 3 See [Table 28](#) and [Table 29](#) for POWER\_GOOD output signal status change.

### 8.4.3 Mask Registers

For each real time Status Registers (Table 112, Register 0x08 [6:2,0], Table 113, Register 0x09 [7,5,3:0], Table 114, Register 0x0A [7:1], Table 115, Register 0x0B [7:0], Table 155, Register 0x33 [3:2]), the PMIC offers a way to mask the status of each event interrupt. The mask registers are Table 125, Register 0x15 [7,5:0], Table 126, Register 0x16 [7,5,3:0], Table 127, Register 0x17 [7:2], Table 128, Register 0x18 [7:0], and Table 129, Register 0x19 [3:2], respectively. The mask registers only mask the event interrupt on GSI\_n and PWR\_GOOD signal. It does not mask the actual status in the register.

There is also global mask register bits control Table 151, Register 0x2F [1:0] to control the GSI\_n and PWR\_GOOD output signal. When all mask registers (Table 125, Register 0x15 [7,5:0], Table 126, Register 0x16 [7,5,3:0], Table 127, Register 0x17 [7:2], Table 128, Register 0x18 [7:0], and Table 129, Register 0x19 [3:2]) are configured as '0', the setting in Table 151, Register 0x2F [1:0] does not matter. The setting Table 151, Register 0x2F [1:0] only matters when one or more mask registers (Table 125, Register 0x15 [7,5:0], Table 126, Register 0x16 [7,5,3:0], Table 127, Register 0x17 [7:2], Table 128, Register 0x18 [7:0], and Table 129, Register 0x19 [3:2]) are configured as '1'.

For any failure events that causes the PMIC to generate VR Disable command on its own, the mask register bits (Table 125, Register 0x15 [0], Table 127, Register 0x17 [7:4], Table 128, Register 0x18 [3:0], Table 129, Register 0x19 [3], and Table 151, Register 0x2F [1:0]) do not apply and PMIC always asserts PWR\_GOOD output signal regardless of the setting in mask registers. The PMIC still updates the status registers appropriately when any event occurs. When masked, the host is expected to read the status registers periodically to learn if any of the events have occurred or not. The host can mask or unmask each event individually. The host can mask or unmask at any time in programmable mode. In secure mode of operation, the mask registers are locked.

**Table 125 — Register 0x15**

R15			
Bits	Attribute	Default	Description
7	RW	0	R15 [7]: MASK_VIN_BULK_INPUT_POWER_GOOD_STATUS Mask VIN_Bulk Input Power Good Status Event <sup>[1]</sup> 0 = Do Not Mask VIN_Bulk Input Power Good Status Event 1 = Mask VIN_Bulk Input Power Good Status Event
6	RV	0	R15 [6]: Reserved
5	RW	1	R15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power Good Status Event <sup>1</sup> 0 = Do Not Mask SWA Output Power Good Status Event 1 = Mask SWA Output Power Good Status Event
4	RW	1	R15 [4]: MASK_SWD_OUTPUT_POWER_GOOD_STATUS Mask SWD Output Power Good Status Event <sup>1</sup> 0 = Do Not Mask SWD Output Power Good Status Event 1 = Mask SWD Output Power Good Status Event
3	RW	1	R15 [3]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power Good Status Event <sup>1</sup> 0 = Do Not Mask SWB Output Power Good Status Event 1 = Mask SWB Output Power Good Status Event
2	RW	1	R15 [2]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power Good Status Event <sup>1</sup> 0 = Do Not Mask SWC Output Power Good Status Event 1 = Mask SWC Output Power Good Status Event
1	RV	0	R15 [1]: Reserved
0	RW	0	R15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Over Voltage Status Event <sup>[2]</sup> 0 = Do Not Mask VIN_Bulk Input Supply Over Voltage Status Event 1 = Mask VIN_Bulk Input Supply Over Voltage Status Event

NOTE 1 Not assert GSI\_n or assert PWR\_GOOD output signal.

NOTE 2 Not assert GSI\_n output signal.

## 8.4.3 Mask Registers (cont'd)

Table 126 — Register 0x16

R16			
Bits	Attribute	Default	Description
7	RW	0	R16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event <sup>[1]</sup>
6	RV	0	R16 [6]: Reserved
5	RW	1	R16 [5]: MASK_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.8V Output Power Good Status Event. 0 = Do Not Mask 1.8V Output Power Good Status Event 1 = Mask 1.8V Output Power Good Status Event <sup>[2]</sup>
4	RV	0	R16 [4]: Reserved
3	RW	0	R16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWA High Output Current Consumption Warning Status Event 0 = Do Not Mask SWA High Output Current Consumption Warning Status Event 1 = Mask SWA High Output Current Consumption Warning Status Event <sup>[1]</sup>
2	RW	0	R16 [2]: MASK_SWD_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWD High Output Current Consumption Warning Status Event 0 = Do Not Mask SWD High Output Current Consumption Warning Status Event 1 = Mask SWD High Output Current Consumption Warning Status Event <sup>[1]</sup>
1	RW	0	R16 [1]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWB High Output Current Consumption Warning Status Event 0 = Do Not Mask SWB High Output Current Consumption Warning Status Event 1 = Mask SWB High Output Current Consumption Warning Status Event <sup>[1]</sup>
0	RW	0	R16 [0]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Mask SWC High Output Current Consumption Warning Status Event 0 = Do Not Mask SWC High Output Current Consumption Warning Status Event 1 = Mask SWC High Output Current Consumption Warning Status Event <sup>[1]</sup>

NOTE 1 Not assert GSI\_n output signal.

NOTE 2 Not assert GSI\_n or assert PWR\_GOOD output signal.

### 8.4.3 Mask Registers (cont'd)

**Table 127 — Register 0x17**

R17			
Bits	Attribute	Default	Description
7	RW	0	R17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask SWA Output Over Voltage Status Event 0 = Do Not Mask SWA Output Over Voltage Status Event 1 = Mask SWA Output Over Voltage Status Event <sup>[1]</sup>
6	RW	0	R17 [6]: MASK_SWD_OUTPUT_OVER_VOLTAGE_STATUS Mask SWD Output Over Voltage Status Event 0 = Do Not Mask SWD Output Over Voltage Status Event 1 = Mask SWD Output Over Voltage Status Event <sup>[1]</sup>
5	RW	0	R17 [5]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask SWB Output Over Voltage Status Event 0 = Do Not Mask SWB Output Over Voltage Status Event 1 = Mask SWB Output Over Voltage Status Event <sup>[1]</sup>
4	RW	0	R17 [4]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask SWC Output Over Voltage Status Event 0 = Do Not Mask SWC Output Over Voltage Status Event 1 = Mask SWC Output Over Voltage Status Event <sup>[1]</sup>
3	RW	0	R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n Output Only <sup>[2]</sup> 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n Output Only <sup>[3]</sup> 0 = Do Not Mask Parity Error Status Event 1 = Mask Parity Error Status
1:0	RV	0	R17 [1:0]: Reserved

NOTE 1 Not assert GSI\_n output signal.

NOTE 2 Only applicable when PMIC is in I3C Basic Mode. This mask register only masks the GSI\_n output signal. Does not apply to IBI.

NOTE 3 Only applicable when PMIC is in I3C Basic Mode or for supported CCC in I<sup>2</sup>C mode. This mask register only masks the GSI\_n output signal. Does not apply to IBI.

### 8.4.3 Mask Registers (cont'd)

**Table 128 — Register 0x18**

R18			
Bits	Attribute	Default	Description
7	RW	0	R18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWA Output Current Limiter Warning Status Event 0 = Do Not Mask SWA Output Current Limiter Warning Status Event 1 = Mask SWA Output Current Limiter Warning Status Event <sup>[1]</sup>
6	RW	0	R18 [6]: MASK_SWD_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWD Output Current Limiter Warning Status Event 0 = Do Not Mask SWD Output Current Limiter Warning Status Event 1 = Mask SWD Output Current Limiter Warning Status Event <sup>[1]</sup>
5	RW	0	R18 [5]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWB Output Current Limiter Warning Status Event 0 = Do Not Mask SWB Output Current Limiter Warning Status Event 1 = Mask SWB Output Current Limiter Warning Status Event <sup>[1]</sup>
4	RW	0	R18 [4]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask SWC Output Current Limiter Warning Status Event 0 = Do Not Mask SWC Output Current Limiter Warning Status Event 1 = Mask SWC Output Current Limiter Warning Status Event <sup>[1]</sup>
3	RW	0	R18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_STATUS Mask SWA Output Under Voltage Status Event 0 = Do Not Mask SWA Output Under Voltage Status Event 1 = Mask SWA Output Under Voltage Status Event <sup>[1]</sup>
2	RW	0	R18 [2]: MASK_SWD_OUTPUT_UNDER_VOLTAGE_STATUS Mask SWD Output Under Voltage Status Event 0 = Do Not Mask SWD Output Under Voltage Status Event 1 = Mask SWD Output Under Voltage Status Event <sup>[1]</sup>
1	RW	0	R18 [1]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_STATUS Mask SWB Output Under Voltage Status Event 0 = Do Not Mask SWB Output Under Voltage Status Event 1 = Mask SWB Output Under Voltage Status Event <sup>[1]</sup>
0	RW	0	R18 [0]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_STATUS Mask SWC Output Under Voltage Status Event 0 = Do Not Mask SWC Output Under Voltage Status Event 1 = Mask SWC Output Under Voltage Status Event <sup>[1]</sup>

NOTE 1 Not assert GSI<sub>n</sub> output signal.



### 8.4.3 Mask Registers (cont'd)

**Table 129 — Register 0x19**

R19			
Bits	Attribute	Default	Description
7:4	RV	0	R19 [7:4]: Reserved
3	RW	0	R19 [3]: MASK_VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS Mask VIN_Bulk Input Under Voltage Lockout Event 0 = Do Not Mask VIN_Bulk Input Under Voltage Lockout 1 = Mask VIN_Bulk Input Under Voltage Lockout <sup>[1]</sup>
2	RW	1	R19 [2]: MASK_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.0V Output Power Good Status Event. <sup>[2]</sup> 0 = Do Not Mask 1.0V Output Power Good Status Event 1 = Mask 1.0V Output Power Good Status Event
1:0	RV	0	R19 [1:0]: Reserved

NOTE 1 Not assert GSI\_n output signal.

NOTE 2 Not assert GSI\_n or PWR\_GOOD output signal.

### 8.4.4 Threshold and Configuration Registers

**Table 130 — Register 0x1A**

R1A			
Bits	Attribute	Default	Description
7:6	RW	10	R1A [7:6]: VIN_BULK_POWER_GOOD_THRESHOLD_VOLTAGE VIN_Bulk Input Threshold Voltage for Input Power Good Status for Input supply Voltage <sup>[1]</sup> 00 = Reserved 01 = 4.25V 10 = 3.0V <sup>[2],[3]</sup> 11 = Reserved
5	RV	0	R1A [5]: Reserved
4	RW	1	R1A [4]: QUIESCENT_STATE_EN PMIC Quiescent State Entry Enable <sup>[4]</sup> 0 = Disable 1 = Enable <sup>[5],[6]</sup>
3	RV	0	R1A [3]: Reserved
2	RW	0	R1A [2]: VOUT_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6 V 1 = Reserved
1	RW	0	R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select <sup>[7]</sup> 0 = Report individual power for each rail in R0C, R0D, R0E and R0F 1 = Report total power of each rail in R0C <sup>[8]</sup>
0	RW	0	R1A [0]: VOUT_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = -10% from the setting in <a href="#">Table 199, Register 0x51</a> [2:1] 1 = -15% from the setting in <a href="#">Table 199, Register 0x51</a> [2:1]

NOTE 1 If VIN\_Bulk input voltage is higher than threshold setting, the PMIC continues to operate as normal. If VIN\_Bulk input voltage falls below the threshold setting, the PMIC may continue to operate but updates its PWR\_GOOD status register and asserts GSI\_n, PWR\_GOOD output signal appropriately.

NOTE 2 If VIN\_Bulk input voltage falls below this threshold setting, the PMIC may not guarantee operation.

NOTE 3 If VIN\_Bulk input voltage continues to fall below vendor specific UVLO, the PMIC triggers VR Disable command and executes power down sequence.

NOTE 4 This bit must be configured before issuing VR Enable command unless Unlock\_n pin is intended to be used to unlock the registers.

NOTE 5 VR Disable command (VR\_EN pin transition to low or [Table 154, Register 0x32](#) [7] = '0' (in programmable mode only)) puts PMIC in Quiescent state.

NOTE 6 Simultaneous usage of programmable mode (i.e., [Table 151, Register 0x2F](#) [2] = '1'), PWR\_GOOD as IO (i.e., [Table 154, Register 0x32](#) [5] = '1') and P1 State Enable (i.e., [Table 130, Register 0x1A](#) [4] = '1') is considered an illegal configuration when VR\_EN pin is intended to be used; otherwise it is a valid configuration if VR\_EN command is used on I<sup>2</sup>C/I<sup>3</sup>C Basic bus.

NOTE 7 This register is only applicable if [Table 131, Register 0x1B](#) [6] = '1'.

NOTE 8 Host should only read [Table 116, Register 0x0C](#) [7:0] for total power. The register contents of [Table 117, Register 0x0D](#), [Table 118, Register 0x0E](#), and [Table 119, Register 0x0F](#) may not be valid.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 131 — Register 0x1B**

R1B			
Bits	Attribute	Default	Description
7	RW	0	R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_Bulk Input Over Voltage Threshold Setting 0 = 5.8 V to 6 V (Varies across vendors) 1 = Reserved
6	RW	0	R1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers: <sup>[1]</sup> 1 = Report Power Measurements in registers <sup>1</sup>
5	RV	0	R1B [5]: Reserved
4	RW	0	R1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin <sup>[2]</sup> 0 = Not Masked 1 = Masked
3	RW	0	R1B [3]: GSI_N_PIN_ENABLE Enable GSI_n Pin <sup>[3]</sup> 0 = Disable GSI_n Pin 1 = Enable GSI_n Pin
2:0	RW	101	R1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold <sup>[4]</sup> 000 = Reserved 001 = PMIC temperature $\geq 85^{\circ}\text{C}$ 010 = PMIC temperature $\geq 95^{\circ}\text{C}$ 011 = PMIC temperature $\geq 105^{\circ}\text{C}$ 100 = PMIC temperature $\geq 115^{\circ}\text{C}$ 101 = PMIC temperature $\geq 125^{\circ}\text{C}$ 110 = PMIC temperature $\geq 135^{\circ}\text{C}$ 111 = Reserved

NOTE 1 [Table 116, Register 0x0C](#), [Table 117, Register 0x0D](#), [Table 118, Register 0x0E](#), and [Table 119, Register 0x0F](#).

NOTE 2 Mask POWER\_GOOD output signal for register bits in [Table 125, Register 0x15](#) [7,5:0], [Table 126, Register 0x16](#) [7,5,3:0], [Table 127, Register 0x17](#) [7:4], [Table 128, Register 0x18](#) [7:0], and [Table 129, Register 0x19](#) [3:2]. Mask Register Control [Table 151, Register 0x2F](#) [1:0] still applies when Global PWR\_GOOD output Mask register is set to '1'.

NOTE 3 This register can be used as Global Mask Function for GSI\_n pin. If disabled, this masks the GSI\_n output signal for all register bits in [Table 125, Register 0x15](#) [7,5:0], [Table 126, Register 0x16](#) [7,5,3:0], [Table 127, Register 0x17](#) [7:4], [Table 128, Register 0x18](#) [7:0], and [Table 129, Register 0x19](#) [3:2].

NOTE 4 The tolerance of the temperature warning threshold is  $\pm 5^{\circ}\text{C}$  from the selected setting.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 132 — Register 0x1C<sup>[1]</sup>**

R1C			
Bits	Attribute	Default	Description
7:0	RW	1111 0000	R1C [7:0]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold <sup>[2]</sup>  If <a href="#">Table 154, Register 0x32</a> [1:0] = '00': 0000 0000 = Undefined 0000 0001 $\geq$ 125 mA 0000 0010 $\geq$ 250 mA ... 1111 1111 $\geq$ 31.875A  If <a href="#">Table 154, Register 0x32</a> [1:0] = '01': 0000 0000 = Undefined 0000 0001 $\geq$ 31.25 mA 0000 0010 $\geq$ 62.5 mA 0000 0011 $\geq$ 93.75 mA 0000 0100 $\geq$ 125 mA ... 1111 1111 $\geq$ 7.968 A

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 207, Register 0x67](#).

NOTE 2 The default value is set based on [Table 154, Register 0x32](#) [1:0] = '01'

**Table 133 — Register 0x1D<sup>[1]</sup>**

R1D			
Bits	Attribute	Default	Description
7:0	RW	0010 0111	R1D [7:0]: SWD_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node D Output High Current Consumption Warning Threshold <sup>[2]</sup>  If <a href="#">Table 154, Register 0x32</a> [1:0] = '00': 0000 0000 = Undefined 0000 0001 $\geq$ 125 mA 0000 0010 $\geq$ 250 mA ... 1111 1111 $\geq$ 31.875A  If <a href="#">Table 154, Register 0x32</a> [1:0] = '01': 0000 0000 = Undefined 0000 0001 $\geq$ 31.25 mA 0000 0010 $\geq$ 62.5 mA 0000 0011 $\geq$ 93.75 mA 0000 0100 $\geq$ 125 mA ... 1111 1111 $\geq$ 7.968 A

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 208, Register 0x68](#).

NOTE 2 The default value is set based on [Table 154, Register 0x32](#) [1:0] = '01'

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 134 — Register 0x1E<sup>[1]</sup>**

R1E			
Bits	Attribute	Default	Description
7:0	RW	0010 0111	<p>R1E [7:0]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold<sup>[2]</sup></p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '00':  0000 0000 = Undefined  0000 0001 <math>\geq</math> 125 mA  0000 0010 <math>\geq</math> 250 mA  ...  1111 1111 <math>\geq</math> 31.875A</p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '01':  0000 0000 = Undefined  0000 0001 <math>\geq</math> 31.25 mA  0000 0010 <math>\geq</math> 62.5 mA  0000 0011 <math>\geq</math> 93.75 mA  0000 0100 <math>\geq</math> 125 mA  ...  1111 1111 <math>\geq</math> 7.968 A</p>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 209, Register 0x69](#).

NOTE 2 The default value is set based on [Table 154, Register 0x32](#) [1:0] = '01'

**Table 135 — Register 0x1F<sup>[1]</sup>**

R1F			
Bits	Attribute	Default	Description
7:0	RW	0010 0000	<p>R1F [7:0]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold<sup>[2]</sup></p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '00':  0000 0000 = Undefined  0000 0001 <math>\geq</math> 125 mA  0000 0010 <math>\geq</math> 250 mA  ...  1111 1111 <math>&gt;</math> 31.875A</p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '01':  0000 0000 = Undefined  0000 0001 <math>\geq</math> 31.25 mA  0000 0010 <math>\geq</math> 62.5 mA  0000 0011 <math>\geq</math> 93.75 mA  0000 0100 <math>\geq</math> 125 mA  ...  1111 1111 <math>\geq</math> 7.968 A</p>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 210, Register 0x6A](#).

NOTE 2 The default value is set based on [Table 154, Register 0x32](#) [1:0] = '01'

#### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 136 — Register 0x20<sup>[1]</sup>**

R20			
Bits	Attribute	Default	Description
7:6	RW	0	R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, lvalley_limit: 00 = 7.5. A 01 = 8.5 A 10 = 9.5 A 11 = Vendor specific
5:4	RW	0	R20 [5:4]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, lvalley_limit: 00 = 0.5 A 01 = 1.0 A 10 = 1.5A 11 = Vendor specific
3:2	RW	0	R20 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, lvalley_limit: 00 = 0.5 A 01 = 1.0 A 10 = 1.5A 11 = Vendor specific
1:0	RW	0	R20 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, lvalley_limit: 00 = 0.5 A 01 = 1.0 A 10 = Reserved 11 = Vendor specific

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 198, Register 0x50](#).

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 137 — Register 0x21<sup>[1],[2]</sup>**

R21			
Bits	Attribute	Default	Description
7:1	RW	011 0010	R21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting <sup>[3],[4]</sup> 000 0000 = 800 <sup>[5]</sup> mV or 800 <sup>[6]</sup> mV 000 0001 = 805 mV or 810 mV 000 0010 = 810 mV or 820 mV ... 011 0010 = 1050 mV or 1300 mV ... 111 1101 = 1425 mV or 2050 mV 111 1110 = 1430 mV or 2060 mV 111 1111 = 1435 mV or 2070 mV
0	RW	0	R21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 1 = -7.5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 187, Register 0x45](#).

NOTE 2 If required, the host must update the settings in register [Table 137, Register 0x21, \[0\]](#), [Table 138, Register 0x22, \[7:2\]](#), and [Table 136, Register 0x20 \[7:6\]](#) first prior to updating the settings in the register [Table 137, Register 0x21, \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1000 mV to 1100 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent false error trigger, the PMIC internally will increment the SWA output voltage setting by 5 or 10 mV at a time. The time it takes for PMIC to adjust the output voltage is 5  $\mu$ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50  $\mu$ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32 \[5\] = '1'](#).

NOTE 5 [Table 147, Register 0x2B, \[5\] = '0'](#); 5 mV step size.

NOTE 6 [Table 147, Register 0x2B, \[5\] = '1'](#); 10 mV step size.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 138 — Register 0x22<sup>[1],[2]</sup>**

R22			
Bits	Attribute	Default	Description
7:6	RW	01	R22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 01 = +7.5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 10 = +10% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 11 = Reserved
5:4	RW	10	R22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over Voltage Status <sup>[3]</sup> 00 = +7.5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 01 = +10% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 10 = +12.5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 11 = Reserved
3:2	RW	00	R22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 01 = -12.5% from the setting in <a href="#">Table 137, Register 0x21, [7:1]</a> 10 = Reserved 11 = Reserved
1:0	RW	00	R22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft Stop Time After VR Disable <sup>[4]</sup> . The register <a href="#">Table 158, Register 0x36 [7]</a> (MSB) plus this two bit register makes the 3 bit encoding. 000 = 0.5 ms 001 = 1 ms 010 = 2 ms 011 = 4 ms 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 188, Register 0x46](#).

NOTE 2 If required, the host must update the setting in register [Table 137, Register 0x21, \[0\]](#), [Table 138, Register 0x22, \[7:2\]](#), and [Table 136, Register 0x20 \[7:6\]](#) first prior to updating the settings in the register [Table 137, Register 0x21, \[7:1\]](#).

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 138, Register 0x22, \[7:6\]](#).

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.



## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 139 — Register 0x23<sup>[1],[2]</sup>**

R23			
Bits	Attribute	Default	Description
7:1	RW	001 0100	R23 [7:1]: SWD_VOLTAGE_SETTING Switch Node D Output Regulator Voltage Setting <sup>[3],[4]</sup> 000 0000 = 800 <sup>[5]</sup> mV or 800 <sup>[6]</sup> mV 000 0001 = 805 mV or 810 mV 000 0010 = 810 mV or 820 mV ... 001 0100 = 900 mV or 1000 mV ... 111 1101 = 1425 mV or 2050 mV 111 1110 = 1430 mV or 2060 mV 111 1111 = 1435 mV or 2070 mV
0	RW	0	R23 [0]: SWD_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 1 = -7.5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 189, Register 0x47](#).

NOTE 2 If required, the host must update the settings in register [Table 139, Register 0x23, \[0\]](#), [Table 140, Register 0x24 \[7:2\]](#), and [Table 136, Register 0x20 \[5:4\]](#) first prior to updating the settings in the register [Table 139, Register 0x23, \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 850 mV to 950 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent false error trigger, the PMIC internally will increment the SWA output voltage setting by 5 or 10 mV at a time. The time it takes for PMIC to adjust the output voltage is 5  $\mu$ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50  $\mu$ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32 \[5\]](#) = '1'.

NOTE 5 [Table 147, Register 0x2B, \[4\]](#) = '0'; 5 mV step size.

NOTE 6 [Table 147, Register 0x2B, \[4\]](#) = '1'; 10 mV step size.

### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 140 — Register 0x24<sup>[1]</sup>**

R24			
Bits	Attribute	Default	Description
7:6	RW	01	R24 [7:6]: SWD_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 01 = +7.5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 10 = +10% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 11 = Reserved
5:4	RW	10	R24 [5:4]: SWD_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Over Voltage Status <sup>[2]</sup> 00 = +7.5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 01 = +10% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 10 = +12.5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 11 = Reserved
3:2	RW	00	R24 [3:2]: SWD_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 01 = -12.5% from the setting in <a href="#">Table 139, Register 0x23, [7:1]</a> 10 = Reserved 11 = Reserved
1:0	RW	00	R24 [1:0]: SWD_OUTPUT_SOFT_STOP_TIME SWD Output Regulator Soft Stop Time After VR Disable <sup>[3]</sup> . The register <a href="#">Table 158, Register 0x36 [6]</a> (MSB) plus this two bit register makes the 3 bit encoding. 000 = 0.5 ms 001 = 1 ms 010 = 2 ms 011 = 4 ms 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 190, Register 0x48](#).

NOTE 2 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 138, Register 0x22, \[7:6\]](#).

NOTE 3 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 141 — Register 0x25<sup>[1],[2]</sup>**

R25			
Bits	Attribute	Default	Description
7:1	RW	011 1100	R25 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting <sup>[3],[4]</sup> 000 0000 = 200 <sup>[5]</sup> mV or 200 <sup>[6]</sup> mV 000 0001 = 205 mV or 202.5 mV 000 0010 = 210 mV or 205 mV ... 011 1100 = 500 mV or 350 mV ... 111 1101 = 825 mV or 512.5 mV 111 1110 = 830 mV or 515 mV 111 1111 = 835 mV or 517.5 mV
0	RW	0	R25 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 1 = -7.5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 191, Register 0x49](#).

NOTE 2 If required, the host must update the settings in register [Table 141, Register 0x25, \[0\]](#), [Table 142, Register 0x26, \[7:2\]](#), and [Table 136, Register 0x20 \[3:2\]](#) first prior to updating the settings in the register [Table 141, Register 0x25, \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 450 mV to 550 mV or from 300 mV to 400 mV depending on the range selection.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However to prevent false error trigger, the PMIC internally will increment the SWB output voltage setting by 5 or 2.5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5  $\mu$ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50  $\mu$ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32 \[5\]](#) = '1'.

NOTE 5 [Table 147, Register 0x2B, \[3\]](#) = '0'; 5 mV step size.

NOTE 6 [Table 147, Register 0x2B, \[3\]](#) = '1'; 2.5 mV step size.

### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 142 — Register 0x26<sup>[1],[2]</sup>**

R26			
Bits	Attribute	Default	Description
7:6	RW	01	R26 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 01 = +7.5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 10 = +10% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 11 = Reserved
5:4	RW	10	R26 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over Voltage Status <sup>[3]</sup> 00 = +7.5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 01 = +10% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 10 = +12.5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 11 = Reserved
3:2	RW	00	R26 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 01 = -12.5% from the setting in <a href="#">Table 141, Register 0x25, [7:1]</a> 10 = Reserved 11 = Reserved
1:0	RW	00	R26 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft Stop Time After VR Disable <sup>[4]</sup> . The register <a href="#">Table 158, Register 0x36 [5]</a> (MSB) plus this two bit register makes the 3 bit encoding. 000 = 0.5 ms 001 = 1 ms 010 = 2 ms 011 = 4 ms 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 192, Register 0x4A](#).

NOTE 2 If required, the host must update the settings in register [Table 141, Register 0x25, \[0\]](#), [Table 142, Register 0x26, \[7:2\]](#), and [Table 136, Register 0x20 \[3:2\]](#) first prior to updating the settings in the register [Table 141, Register 0x25, \[7:1\]](#).

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 142, Register 0x26, \[7:6\]](#).

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 143 — Register 0x27<sup>[1],[2]</sup>**

R27			
Bits	Attribute	Default	Description
7:1	RW	011 1100	R27 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting <sup>[3],[4]</sup> 000 0000 = 1500 <sup>[5]</sup> mV or 1500 <sup>[6]</sup> mV 000 0001 = 1505 mV or 1510 mV 000 0010 = 1510 mV or 1520 mV ... 011 1100 = 1800 mV or 2100 mV ... 111 1101 = 2125 mV or 2750 mV 111 1110 = 2130 mV or 2760 mV 111 1111 = 2135 mV or 2770 mV
0	RW	0	R27 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 1 = -7.5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 193, Register 0x4B](#).

NOTE 2 If required, the host must update the settings in register [Table 143, Register 0x27, \[0\]](#), [Table 144, Register 0x28, \[7:2\]](#), and [Table 136, Register 0x20 \[1:0\]](#) first prior to updating the settings in the register [Table 143, Register 0x27, \[7:1\]](#).

NOTE 3 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1750 mV to 1850 mV.

NOTE 4 After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent false error triggers, the PMIC internally will increment the SWC output voltage setting by 5 or 10 mV at a time. The time it takes for PMIC to adjust the output voltage is 5  $\mu$ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50  $\mu$ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32 \[5\]](#) = '1'.

NOTE 5 [Table 147, Register 0x2B, \[0\]](#) = '0'; 5 mV step size.

NOTE 6 [Table 147, Register 0x2B, \[0\]](#) = '1'; 10 mV step size.

### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 144 — Register 0x28<sup>[1],[2]</sup>**

R28			
Bits	Attribute	Default	Description
7:6	RW	01	R28 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 01 = +7.5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 10 = +10% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 11 = Reserved
5:4	RW	10	R28 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over Voltage Status <sup>[3]</sup> 00 = +7.5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 01 = +10% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 10 = +12.5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 11 = Reserved
3:2	RW	00	R28 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 01 = -12.5% from the setting in <a href="#">Table 143, Register 0x27, [7:1]</a> 10 = Reserved 11 = Reserved
1:0	RW	00	R28 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft Stop Time After VR Disable <sup>[4]</sup> . The register <a href="#">Table 158, Register 0x36 [4]</a> (MSB) plus this two bit register makes the 3 bit encoding. 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 8 ms 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = Vendor defined

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 194, Register 0x4C](#).

NOTE 2 If required, the host must update the settings in register [Table 143, Register 0x27, \[0\]](#), [Table 144, Register 0x28, \[7:2\]](#), and [Table 136, Register 0x20 \[1:0\]](#) first prior to updating the settings in the register [Table 143, Register 0x27, \[7:1\]](#).

NOTE 3 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 144, Register 0x28, \[7:6\]](#).

NOTE 4 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 145 — Register 0x29<sup>[1],[2]</sup>**

R29			
Bits	Attribute	Default	Description
7:6	RW	10	R29 [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R29 [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific
3:2	RW	10	R29 [3:2]: SWD_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	00	R29 [1:0]: SWD_SWITCHING_FREQ Switch Node D Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 195, Register 0x4D](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 154, Register 0x32 \[7\]](#).

### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 146 — Register 0x2A<sup>[1],[2]</sup>**

R2A			
Bits	Attribute	Default	Description
7:6	RW	10	R2A [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R2A [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific
3:2	RW	10	R2A [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	00	R2A [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor Specific 10 = Vendor Specific 11 = Vendor Specific

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 196, Register 0x4E](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 154, Register 0x32 \[7\]](#).



## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 147 — Register 0x2B<sup>[1],[2]</sup>**

R2B			
Bits	Attribute	Default	Description
7:6	RW	01	R2B [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting <sup>[3]</sup> 00 = 1.7 V 01 = 1.8 V 10 = 1.9 V 11 = 2.0 V
5	RW	0	R2B [5]: SWA_VOLTAGE_STEP_SIZE SWA Voltage Step Size 0 = 5 mV 1 = 10 mV
4	RW	0	R2B [4]: SWD_VOLTAGE_STEP_SIZE SWD Voltage Step Size 0 = 5 mV 1 = 10 mV
3	RW	0	R2B [3]: SWB_VOLTAGE_STEP_SIZE SWB Voltage Step Size 0 = 5 mV 1 = 2.5 mV
2:1	RW	01	R2B [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting <sup>[4]</sup> 00 = 0.9 V 01 = 1.0 V 10 = 1.1 V 11 = 1.2 V
0	RW	0	R2B [0]: SWC_VOLTAGE_STEP_SIZE SWC Voltage Step Size 0 = 5 mV 1 = 10 mV

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 199, Register 0x51](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 154, Register 0x32](#) [7].  
The host must also wait minimum of 5  $\mu$ s after the adjustment before issuing VR Enable command.

NOTE 3 The VOUT\_1.8V Power Good threshold in register [Table 130, Register 0x1A](#) [2] is always fixed regardless of the setting in this register.

NOTE 4 If required, the host must adjust this register one step at a time (0.1 V increment or decrement) to prevent false trigger of power good status and PWR\_GOOD pin assertion. In other words, host should not increment or decrement 0.2 V or 0.3 V from its current setting.

### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 148 — Register 0x2C<sup>[1],[2]</sup>**

R2C			
Bits	Attribute	Default	Description
7:5	RW	001	R2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft Start Time After VR Enable <sup>[3]</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4	RV	0	R2C [4]: Reserved
3:1	RW	001	R2C [3:1]: SWD_OUTPUT_SOFT_START_TIME SWD Output Regulator Soft Start Time After VR Enable <sup>[4]</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
0	RV	0	R2C [0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 204, Register 0x5D](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 154, Register 0x32 \[7\]](#).

NOTE 3 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

NOTE 4 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 149 — Register 0x2D<sup>[1],[2]</sup>**

R2D			
Bits	Attribute	Default	Description
7:5	RW	001	R2D [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft Start Time After VR Enable <sup>[3]</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4	RV	0	R2D [4]: Reserved
3:1	RW	001	R2D [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft Start Time After VR Enable <sup>3</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
0	RW	0	R2D [0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 205, Register 0x5E](#).

NOTE 2 If required, the host must adjust this register first before issuing VR Enable command in [Table 154, Register 0x32 \[7\]](#).

NOTE 3 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage)

## 8.4.4 Threshold and Configuration Registers (cont'd)

Table 150 — Register 0x2E

R2E			
Bits	Attribute	Default	Description
7:6	RW	11	R2E [7:6]: SWB_DVFSQ_VOLTAGE_SLEW_RATE SWB Output Voltage Slew Rate when transitioning from P3 to DVFSQ and DVFSQ to P3 state <sup>[1],[2]</sup> 00 = 15 mV/μs 01 = 10 mV/μs 10 = 5 mV/μs 11 = 1 mV/μs
5	RW	1	R2E [5]: SWB_DISABLE_INPUT_PIN_ENABLE SWB_Disable Input Pin Enable <sup>[3]</sup> 0 = Disable; Input pin receiver is disabled 1 = Enable; Input pin receiver is enabled
4	RW	0	R2E [4]: DVFSQ_N_PIN_ENABLE DVFSQ_n Input Pin Enable <sup>[4]</sup> 0 = Disable; SWB output voltage setting is as configured in register <a href="#">Table 141, Register 0x25, [7:1]</a> , <a href="#">Table 147, Register 0x2B, [3]</a> . 1 = Enable <sup>[2]</sup> ; SWB output voltage setting toggles between register <a href="#">Table 141, Register 0x25, [7:1]</a> , <a href="#">Table 147, Register 0x2B, [3]</a> and register <a href="#">Table 166, Register 0x3E, [7:1]</a> , <a href="#">Table 147, Register 0x2B, [3]</a> depending on DVFSQ_n input pin transition.
3	RW	1	R2E [3]: UNLOCK_PIN_ENABLE Unlock Input Pin Enable <sup>[5],[6]</sup> 0 = Disable; the input receiver is off and pin has no effect. 1 = Enable; When Unlock pin is high, the PMIC is in programmable mode ( <a href="#">Table 151, Register 0x2F [2] = '1'</a> ); when Unlock pin is low, the PMIC is in secure mode ( <a href="#">Table 151, Register 0x2F [2] = '0'</a> ).
2:0	RW	100	R2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature ≥ 105 °C 001 = PMIC Temperature ≥ 115 °C 010 = PMIC Temperature ≥ 125 °C 011 = PMIC Temperature ≥ 135 °C 100 = PMIC Temperature ≥ 145 °C 101 = Reserved 110 = Reserved 111 = Reserved

NOTE 1 At first power on, this bit is automatically configured identically by PMIC on its own as [Table 206, Register 0x5F \[2:1\]](#).

NOTE 2 During the SWB output voltage transition, the PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting and keeps the PWR\_GOOD signal Hi-Z. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32 \[5\] = '1'](#).

NOTE 3 At first power on, this bit is automatically configured identically by PMIC on its own as [Table 186, Register 0x44 \[0\]](#).

NOTE 4 This register cannot be cleared by the controller when [Table 114, Register 0x0A \[0\] = '1'](#).

NOTE 5 At first power on, this bit is automatically configured identically by PMIC on its own as [Table 206, Register 0x5F \[3\]](#).

NOTE 6 This register is automatically cleared to '0' by PMIC when it enters the Locked security state.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 151 — Register 0x2F**

R2F			
Bits	Attribute	Default	Description
7	RV	0	R2F [7]: Reserved
6	RW	0	R2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output <sup>[1],[2]</sup> 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RW	0	R2F [5]: SWD_REGULATOR_CONTROL Disable SWD Regulator Output <sup>[1],[2]</sup> 0 = Disable Switch Node D Output Regulator 1 = Enable Switch Node D Output Regulator
4	RW	0	R2F [4]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output <sup>[1],[2]</sup> 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RW	0	R2F [3]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output <sup>[1],[2]</sup> 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2	RW	0	R2F [2]: SECURE_MODE PMIC Mode Operation <sup>[3]</sup> 0 = Secure Mode Operation <sup>[4],[5],[6]</sup> 1 = Programmable Mode Operation
1:0	RW	10	R2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control <sup>[7]</sup> 00 = Mask GSI_n Signal Only (PWR_GOOD Signal asserts) 01 = Mask PWR_GOOD Signal Only (GSI_n Signal asserts) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD asserts nor GSI_n asserts) 11 = Reserved

NOTE 1 This bit must be used only after power up sequence (after VR Enable command). At first power up, PMIC automatically updates the status of this register to '1' after VR Enable command. When VR Enable command is registered, the PMIC updates this register based on Power On Sequence Configuration (0 to 3) setting. If enabled in Power On Sequence Configuration 0 to 3 registers, only then, under programmable mode of operation, the PMIC's output regulator can be disabled by clearing this bit and they can be re-enabled again by setting this bit. The PMIC does not alter its Power Good output signal and keeps it asserted High. If any regulator is not enabled in Power on Sequence Configuration 0 to 3, it cannot be enabled using this register. For example, if only SWA is enabled and SWB and SWC are not enabled in [Table 182, Register 0x40 \[7:0\]](#) to [Table 185, Register 0x43 \[7:0\]](#), then only SWA can be disabled and then re-enabled again but SWB and SWC cannot be enabled using [Table 151, Register 0x2F \[6:3\]](#).

NOTE 2 In programmable mode, after VR enable command, if any output regulators are disabled by clearing [Table 151, Register 0x2F \[6:3\]](#) and then if host issues VR Disable command or PMIC internally triggers VR Disable command, the PMIC keeps the disabled output regulator in [Table 151, Register 0x2F \[6:3\]](#) off and remaining output regulators are disabled by following the Power Off Sequence Configuration 0 to 3 settings.

NOTE 3 At first power on, this register is automatically configured identically by PMIC on its own as [Table 206, Register 0x5F \[7\]](#).

- NOTE 4 This bit must be configured before issuing VR Enable command. If this bit is configured to '0', when PMIC registers VR Enable command, all registers bits starting [Table 125, Register 0x15](#) to [Table 151, Register 0x2F](#), [Table 154, Register 0x32](#) [7,5:0] in host region as well as [Table 182, Register 0x40](#) to Register 0x6F in the CAMM2 vendor region are secured and host cannot change unless the PMIC goes through power cycle.
- NOTE 5 Simultaneous usage of programmable mode (i.e., [Table 151, Register 0x2F](#) [2] = '1'), PWR\_GOOD as IO (i.e., [Table 154, Register 0x32](#) [5] = '1'), and P1 State Enable (i.e., [Table 130, Register 0x1A](#) [4] = '1') is considered an illegal configuration when VR\_EN pin is intended to be used; otherwise it is a valid configuration if VR\_EN command is used on I<sup>2</sup>C/I<sup>3</sup>C Basic bus.
- NOTE 6 When Unlock pin is enabled, the PMIC sets this register to '1' when the Unlock input is high and '0' when the Unlock input is low.
- NOTE 7 Applies to Mask Registers [Table 125, Register 0x15](#) [5:2,0], [Table 126, Register 0x16](#) [7,5,3:0], [Table 127, Register 0x17](#) [7:2], [Table 128, Register 0x18](#) [7:0], and [Table 129, Register 0x19](#) [2] when any one or more Mask registers are set to '1'. If all Mask registers are configured as '0', the setting in this register ([Table 151, Register 0x2F](#) [1:0]) does not apply.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 152 — Register 0x30**

R30			
Bits	Attribute	Default	Description
7	RW	0	R30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable <sup>[1]</sup> 1 = Enable
6:3	RW	0	R30 [6:3]: ADC_SELECT Input Selection for ADC Readout <sup>[2]</sup> 0000 = SWA Output Voltage 0001 = SWD Output Voltage 0010 = SWB Output Voltage 0011 = SWC Output Voltage 0100 = Reserved 0101 = VIN_Bulk Input Voltage 0110 = Reserved 0111 = Reserved 1000 = VOUT_1.8V Output Voltage 1001 = VOUT_1.0V Output Voltage 1111 = VBIAS Output Voltage All other encodings are reserved.
2	RW	0	R30 [2]: REGISTER_ADDRESSING_MODE Register Addressing for I <sup>2</sup> C and I <sup>3</sup> C Protocol <sup>[3]</sup> 0 = 1 Byte address; Configuration register space limited to 256 Bytes 1 = 2 Byte address; Configuration register space up to 64K Bytes
1:0	RW	0	R30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency <sup>[4],[5]</sup> 00 = 1 ms 01 = 2 ms 10 = 4 ms 11 = 8 ms

NOTE 1 Disables the ADC function completely. Applies to voltage readout in [Table 153, Register 0x31 \[7:0\]](#), as well as current or power readout in [Table 116, Register 0x0C \[7:0\]](#), [Table 117, Register 0x0D \[7:0\]](#), [Table 118, Register 0x0E \[7:0\]](#), [Table 119, Register 0x0F \[7:0\]](#), [Table 168, Register 0x100 \[7:0\]](#), [Table 169, Register 0x102 \[7:0\]](#), [Table 170, Register 0x103 \[7:0\]](#), [Table 171, Register 0x104 \[7:0\]](#), and [Table 172, Register 0x105 \[7:0\]](#). When ADC is disabled, the PMIC does not report warning status in [Table 113, Register 0x09 \[3:0\]](#) as [Table 132, Register 0x1C \[7:0\]](#) to [Table 135, Register 0x1F \[7:0\]](#) does not apply. The ADC disable function does not apply to thermal sensor temperature readout in [Table 155, Register 0x33 \[7:5\]](#) as well as high temperature warning and critical temperature shutdown.

NOTE 2 The host shall wait minimum of 9 ms delay after the input selection for ADC readout and the actual readout from [Table 153, Register 0x31](#) to get the latest reading.

NOTE 3 When there is a change in addressing mode, STOP operation is required on I<sup>2</sup>C or I<sup>3</sup>C bus.

NOTE 4 For average output current or power measurement in registers [Table 116, Register 0x0C \[7:0\]](#), [Table 117, Register 0x0D \[7:0\]](#), [Table 118, Register 0x0E \[7:0\]](#), and [Table 119, Register 0x0F \[7:0\]](#).

NOTE 5 This register represents how often the registers are updated. The internal sampling rate is vendor specific.

### 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 153 — Register 0x31**

R31			
Bits	Attribute	Default	Description
7:0	RO	0	<p>R31 [7:0]: ADC_READ</p> <p>ADC Output Voltage Reading<sup>[1]</sup> (Applies to SW[A:D], VOUT_1.8V, VOUT_1.0V)</p> <p>0000 0000 = Undefined</p> <p>0000 0001 = 15 mV</p> <p>0000 0010 = 30 mV</p> <p>..</p> <p>1111 1111 &gt; = 3825 mV</p> <p>ADC Output Voltage Reading<sup>[2]</sup> (Applies to VIN_Bulk Input Voltage)</p> <p>0000 0000 = Undefined</p> <p>0000 0001 = 70 mV</p> <p>0000 0010 = 140 mV</p> <p>..</p> <p>1111 1111 &gt; = 17850 mV</p> <p>ADC Output Voltage Reading<sup>[3]</sup> (Applies to VBias output Voltage)</p> <p>0000 0000 = Undefined</p> <p>0000 0001 = 25 mV</p> <p>0000 0010 = 50 mV</p> <p>..</p> <p>1111 1111 &gt; = 6375 mV</p>

NOTE 1 Only valid when Table 152, Register 0x30 [6:3] = '0000' or '0001' or '0010' or '0011' or '1000' or '1001'.

NOTE 2 Only valid when Table 152, Register 0x30 [6:3] = '0101'.

NOTE 3 Only valid when Table 152, Register 0x30 [6:3] = '1111'.



## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 154 — Register 0x32**

R32			
Bits	Attribute	Default	Description
7	RW	0	R32 [7]: VR_ENABLE PMIC Enable <sup>[1],[2],[3],[4]</sup> 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection <sup>[5]</sup> 0 = I <sup>2</sup> C Protocol (Max speed 1 MHz) 1 = I3C Basic Protocol
5	RW	0	R32 [5]: PWR_GOOD_IO_TYPE PMIC PWR_GOOD Output Signal Type <sup>[6]</sup> 0 = Output Only 1 = Input and Output <sup>[7]</sup>
4:3	RW	0	R32 [4:3]: PWR_GOOD_OUTPUT_SIGNAL_CONTROL PMIC PWR_GOOD Output Signal Control 0x = PMIC controls PWR_GOOD on its own based on internal status 10 = PWR_GOOD Output Low 11 = PWR_GOOD Output Floats <sup>[8]</sup>
2	RV	0	R32 [2]: Reserved
1:0	RW	01	R32 [1:0]: ADC_ACCURACY_STEP_SIZE ADC Accuracy Step Size 00 = 125 mA or 125 mW <sup>[9]</sup> 01 = 31.25 mA or 31.25 mW <sup>[10]</sup> All other encodings are reserved

NOTE 1 The PMIC updates this bit when VR\_EN signal transition to high or when host issues VR Enable command over I<sup>2</sup>C/I3C Basic bus; whichever comes first. PMIC also updates this bit when VR\_EN signal transitions to low or when host issues VR Disable command over I<sup>2</sup>C/I3C Basic bus in programmable mode; whichever comes first. Further, PMIC updates this bit when PWR\_GOOD input is low (if [Table 154, Register 0x32](#) [5] = '1') or when PMIC internally generates VR Disable command due to fault condition regardless of PMIC's VR\_EN signal input status.

NOTE 2 After this bit is set to '1', the PMIC executes Power On Sequence configuration 0 ([Table 182, Register 0x40](#)) to Power On Sequence configuration 3 ([Table 185, Register 0x43](#)) registers. At least one bit in [Table 182, Register 0x40](#) [6:3] must be set to '1' to issue VR Enable (either with VR\_EN pin or over I<sup>2</sup>C/I3C Basic bus) command.

NOTE 3 The host shall ensure that prior to issuing VR Enable command, there is no pending IBI interrupt (i.e., [Table 114, Register 0x0A](#) [1] = '1'). After host issues VR Enable command (either with VR\_EN pin or over I<sup>2</sup>C/I3C Basic bus), the PMIC may NACK any I<sup>2</sup>C or I3C Basic bus transactions by host until tPMIC\_PWR\_GOOD\_OUT timing parameter is satisfied. The host shall not access any device specific registers or issue CCCs until tPMIC\_PWR\_GOOD\_Out parameter is satisfied. The PMIC device may request for an IBI during power up sequence (i.e., during tPMIC\_PWR\_GOOD\_Out time) if there is any event.

NOTE 4 An exception to this register is applied. When PMIC is operating in secure mode of operation and PWR\_GOOD input is low (if [Table 154, Register 0x32](#) [5] = '1'), the PMIC unlocks this register. The PMIC allows host to issue VR Enable command. After host issues VR Enable command, the PMIC re-locks this register.

NOTE 5 This register is automatically updated when SETAASA CCC or RSTDAAC CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in clause 5.4.13 regardless of whether PMIC is in secure mode or programmable mode of operation. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I<sup>2</sup>C mode or I3C Basic mode of operation. When this register is updated, it takes effect when there is a next START operation (i.e., after STOP operation).

NOTE 6 This bit must be configured before issuing VR Enable command.

NOTE 7 Simultaneous usage of programmable mode (i.e., [Table 151, Register 0x2F](#) [2] = '1'), PWR\_GOOD as IO (i.e., [Table 154, Register 0x32](#) [5] = '1'), and P1 State Enable (i.e., [Table 130, Register 0x1A](#) [4] = '1') is considered an illegal configuration when VR\_EN pin is intended to be used; otherwise it is a valid configuration if VR\_EN command is used on I<sup>2</sup>C/I<sup>3</sup>C Basic bus.

NOTE 8 When this encoding is set, the PMIC always floats the PWR\_GOOD output signal even when there is an internal VR Disable command due to fault condition.

NOTE 9 See registers [Table 116, Register 0x0C](#) to [Table 119, Register 0x0F](#) for current or power measurement.

NOTE 10 See registers [Table 168, Register 0x100](#) to [Table 172, Register 0x105](#) for current or power measurement.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 155 — Register 0x33**

R33			
Bits	Attribute	Default	Description
7:5	RO	0	R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature <sup>[1]</sup> 000 = < 85 °C 001 = 85 °C 010 = 95 °C 011 = 105 °C 100 = 115 °C 101 = 125 °C 110 = 135 °C 111 = ≥ 140 °C
4	RV	0	R33 [4]: Reserved
3	RO	0	R33 [3]: VIN_BULK_UNDER_VOLTAGE_LOCKOUT_STATUS VIN_Bulk Under Voltage Lockout Status <sup>[2]</sup> 0 = No Under Voltage Lockout 1 = Under Voltage Lockout
2	RO	0	R33 [2]: VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS VOUT_1.0V LDO Output Power Good Status <sup>[3]</sup> 0 = Power Good 1 = Power Not Good
1	RO	-	R33 [1]: DVFSQ_N_PIN_INPUT_LEVEL_STATUS DVFSQ_n Input Pin Level Status <sup>[4],[5],[6]</sup> 0 = Low 1 = High
0	RO	-	R33 [0]: UNLOCK_PIN_INPUT_LEVEL_STATUS Unlock Pin Input Level Status <sup>[6],[7]</sup> 0 = Low 1 = High

NOTE 1 The accuracy of the temperature readout code is  $\pm 5$  °C.

NOTE 2 This register is set when VIN\_Bulk input voltage goes below 3.0 V (the exact voltage threshold is vendor specific).

NOTE 3 This register is set when VOUT\_1.0V output drops below the threshold setting in register [Table 130, Register 0x1A](#) [0].

NOTE 4 This register status is only applicable if [Table 150, Register 0x2E](#) [4] = '1'. This register bit reflects the voltage level status on the DVFSQ\_n input pin. In the rare event where there is a simultaneous operation of reading this register and DVFSQ\_n pin transition, the PMIC may not reflect the latest status. It is recommended that host performs more than one register read operation to get the latest input pin status.

NOTE 5 This register ([Table 155, Register 0x33](#) [1]) status does not indicate the PMIC DVFSQ Power State Status ([Table 114, Register 0x0A](#) [0]). DVFSQ power state entry is determined by the detection of high to low or low to high voltage edge transition or by VR Disable command (either with VR\_EN pin de-assertion or via I<sup>2</sup>C/I<sup>3</sup>C bus command).

NOTE 6 The controller cannot clear this register via any I<sup>2</sup>C/I<sup>3</sup>C bus command.

NOTE 7 This register status is only applicable if [Table 150, Register 0x2E](#) [3] = '1'. This register bit reflects the voltage level status on the Unlock input pin. In the rare event where there is a simultaneous operation of reading this register and Unlock pin transition, the PMIC may not reflect the latest status. It is recommended that host performs more than one register read operation to get the latest input pin status. If [Table 150, Register 0x2E](#) [3] = '0', this register is always '0'.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 156 — Register 0x34**

R34			
Bits	Attribute	Default	Description <sup>[1]</sup>
7	RO	0	R34 [7]: PEC_ENABLE Packet Error Code Enable <sup>[2]</sup> (Applicable Only if <a href="#">Table 154, Register 0x32</a> [6] = '1') 0 = Disable 1 = Enable
6	RO	0	R34 [6]: IBI_ENABLE In Band Interrupt Enable <sup>[3]</sup> (Applicable Only if <a href="#">Table 154, Register 0x32</a> [6] = '1') 0 = Disable 1 = Enable
5	RO	0	R34 [5]: PARITY_DISABLE T Bit Parity Code Disable <sup>2</sup> (Applicable Only if <a href="#">Table 154, Register 0x32</a> [6] = '1'.) 0 = Enable 1 = Disable <sup>[4]</sup>
4	RV	0	R34 [4]: Reserved
3:1	RO	111	R34 [3:1]: HID_CODE PMIC's 3-bit HID Code <sup>[5]</sup> 000 001 010 011 100 101 110 111
0	RV	0	R34 [0]: Reserved

NOTE 1 The write (or update) transaction to this register must be followed by STOP operation to allow PMIC device to update the setting.

NOTE 2 This register is automatically updated when RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in clause [5.4.13](#). This register cannot be written by the Host through normal write operation either in I<sup>2</sup>C mode or I3C mode of operation. This register is updated with DEVCTRL CCC with RegMod='0' only. This register cannot be written with DEVCTRL CCC with RegMod = '1'.

NOTE 3 This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the PMIC device or when PMIC device goes through bus reset as described in clause [5.4.13](#). This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I<sup>2</sup>C mode or I3C mode of operation. This register cannot be written with DEVCTRL CCC with RegMod = '1'.

NOTE 4 When Parity function is disabled, the PMIC simply ignores the "T" bit information from the Host. The host may actually choose to compute the parity and send that information in "T" bit or simply drive static low or high in "T" bit.

NOTE 5 This register is updated when PMIC device receives SETHID CCC or when PMIC device goes through bus reset as described in clause [5.4.13](#). This register cannot be written with DEVCTRL CCC with RegMod = '1'.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 157 — Register 0x35**

R35			
Bits	Attribute	Default	Description <sup>[1],[2]</sup>
7	RW	0	R35 [7]: ERROR_INJECTION_ENABLE Error Injection Enable <sup>[3]</sup> 0 = Disable 1 = Enable
6:4	RW	0	R35 [6:4]: ERROR_INJECTION_RAIL_SELECTION Error Injection - Input Rail and Output Rail Selection <sup>[4]</sup> 000 = Undefined 001 = SWA Output Only 010 = SWD Output Only 011 = SWB Output Only 100 = SWC Output Only 101 = VIN_Bulk Input Only 110 = Reserved 111 = Do Not Use
3	RW	0	R35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT Over Voltage or Under Voltage Selection for Bits [6:4] <sup>[5]</sup> 0 = Over Voltage 1 = Under Voltage <sup>[6]</sup>
2:0	RW	0	R35[2:0]: MISC_ERROR_INJECTION_TYPE Miscellaneous Error Injection Type <sup>[7]</sup> 000 = Undefined 001 = Reserved 010 = Critical Temperature Shutdown 011 = High Temperature Warning Threshold 100 = VOUT_1.8V LDO Power Good 101 = High Current Consumption Warning <sup>[8]</sup> 110 = Reserved 111 = Current Limiter Warning <sup>9</sup>

NOTE 1 Refer to clause 4.18 for error function usage model. The host can erase the error log registers (Table 108, Register 0x04 to Table 111, Register 0x07) by writing 0x74 to Table 161, Register 0x39.

NOTE 2 To exit from Error Injection Mode, the PMIC must go through power cycle of VIN\_Bulk input supply.

NOTE 3 When error function is invoked by setting bit [7] = '1', the setting of bits [6:4, 2:0] = '000 000' is considered an illegal setting.

NOTE 4 This register Table 157, Register 0x35 [6:4] is only applicable if Table 157, Register 0x35 [2:0] is '000'. Any value other than '000' in both Table 157, Register 0x35 [6:4] and Table 157, Register 0x35 [2:0] is considered an illegal setting and PMIC operation is not guaranteed.

NOTE 5 This register Table 157, Register 0x35 [3] is only applicable if bits [6:4] is anything other than '000'.

NOTE 6 The under voltage selection only applies to SWx output rails and VIN\_Bulk input.

NOTE 7 This register Table 157, Register 0x35 [2:0] is only applicable if Table 157, Register 0x35 [6:3] is '0000'. Any value other than '000' in both Table 157, Register 0x35 [6:4] and Table 157, Register 0x35 [2:0] is considered an illegal setting and PMIC operation is not guaranteed.

NOTE 8 Applies to all enabled SWx output regulators at the same time.

## 8.4.4 Threshold and Configuration Registers (cont'd)

**Table 158 — Register 0x36**

R36			
Bits	Attribute	Default	Description
7	RW	0	R36 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION SWA Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 138, Register 0x22</a> , [1:0] makes 3 bit register encoding. <sup>[1]</sup>
6	RW	0	R36 [6]: SWD_OUTPUT_SOFT_STOP_TIME_EXTENSION SWD Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 140, Register 0x24</a> [1:0] makes 3 bit register encoding. <sup>[2]</sup>
5	RW	0	R36 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION SWB Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 142, Register 0x26</a> , [1:0] makes 3 bit register encoding. <sup>[3]</sup>
4	RW	0	R36 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION SWC Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 144, Register 0x28</a> , [1:0] makes 3 bit register encoding. <sup>[4]</sup>
3:1	RW	001	R36 [3:1]: ACOUSTIC_NOISE_PREVENTION_CONTROL Acoustic Noise Prevention Control Feature 000 = Feature is disabled 001 = Enable; Switching frequency threshold = 50 KHz 010 = Enable; Switching frequency threshold = 40 KHz 011 = Enable; Switching frequency threshold = 30 KHz 100 = Enable; Switching frequency threshold = 20 KHz
0	RV	0	R36 [0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 186, Register 0x44](#) [7].

NOTE 2 At first power on, this register is automatically configured identically by PMIC on its own as [Table 186, Register 0x44](#) [6].

NOTE 3 At first power on, this register is automatically configured identically by PMIC on its own as [Table 186, Register 0x44](#) [5].

NOTE 4 At first power on, this register is automatically configured identically by PMIC on its own as [Table 186, Register 0x44](#) [4].

## 8.4.5 Password Input and Command Code

**Table 159 — Register 0x37**

R37			
Bits	Attribute	Default	Description
7:0	WO	-	R37 [7:0]: CAMM2_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE CAMM2 Vendor Memory Region (0x40 - 0x6F) Password - Lower Byte [7:0] = Code

**Table 160 — Register 0x38**

R38			
Bits	Attribute	Default	Description
7:0	WO	-	R38 [7:0]: CAMM2_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE CAMM2 Vendor Memory Region (0x40 - 0x6F) Password - Upper Byte [7:0] = Code

## 8.4.5 Password Input and Command Code (cont'd)

**Table 161 — Register 0x39**

R39			
Bits	Attribute	Default	Description
7:0	RW	0x00	<p>R39 Codes:</p> <p>Host Region Codes:</p> <p>0x74: Clear Registers R04 to R07, Erase MTP memory for R04 Register to R07.</p> <p>CAMM2 Vendor Region (0x40 to 0x6F) Write Codes:</p> <p>0x40: Unlock CAMM2 Vendor Region. Password needs to be present in R37 &amp; R38 registers.</p> <p>0x00: Lock CAMM2 Vendor Region.</p> <p>0x80: Burn CAMM2 Vendor Region Password. New password needs to be present in R37 &amp; R38.</p> <p>0x81: Burn CAMM2 Vendor Region - 0x40 to 0x4F</p> <p>0x82: Burn CAMM2 Vendor Region - 0x50 to 0x5F</p> <p>0x85: Burn CAMM2 Vendor Region - 0x60 to 0x6F (except for R6D[4,0], R6E[4,0])</p> <p>0x86: Clear CAMM2 Vendor Region Registers: R6D[4,0], R6E[4,0]</p> <p>CAMM2 Vendor Region (0x40 to 0x6F) Read Codes:</p> <p>0x5A: Burning is complete in CAMM2 Vendor region.</p>

## 8.4.6 Miscellaneous Registers

**Table 162 — Register 0x3A**

R3A			
Bits	Attribute	Default	Description <sup>[1]</sup>
7	RV	0	R3A [7]: Reserved
6	RW	0	<p>R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE</p> <p>Enable Default Address Read Pointer when PMIC sees STOP operation</p> <p>0 = Disable Default Address Pointer (address pointer is set by Host)<sup>[2]</sup></p> <p>1 = Enable Default Address Pointer; Address selected by register bits [5:4]</p>
5:4	RW	0	<p>R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS</p> <p>Default Read Address Pointer Selection when PMIC sees STOP operation<sup>[3]</sup></p> <p>00 = R08</p> <p>01 = R0C</p> <p>10 = R100</p> <p>11 = Reserved</p>
3:2	RW	0	<p>R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER</p> <p>Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode<sup>[4]</sup></p> <p>00 = 2 Bytes</p> <p>01 = 4 Bytes</p> <p>10 = 8 Bytes</p> <p>11 = 16 Bytes</p>
1:0	RV	0	R3A [1:0]: Reserved

NOTE 1 The write (or update) transaction to this register must be followed by STOP operation to allow the PMIC device to update the setting.

NOTE 2 The register setting in R3A [5:4] is a don't care.

NOTE 3 This register is only applicable if R3A [6] = '1'.

NOTE 4 This register is only applicable if R3A [6] = '1' and R34 [7] = '1'.

**8.4.6 Miscellaneous Registers (cont'd)****Table 163 — Register 0x3B**

R3B			
Bits	Attribute	Default	Description
7:6	RV	0	R3B [7:6]: Reserved
5:4	ROA	-	R3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROA	-	R3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3 All other encodings are reserved.
0	ROA	1	R3B [0]: PMIC_PART_ID Client PMIC Part ID Identification 0 = PMIC5100 1 = PMIC5200

**Table 164 — Register 0x3C**

R3C			
Bits	Attribute	Default	Description
7:0	ROA	-	R3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0.

**Table 165 — Register 0x3D**

R3D			
Bits	Attribute	Default	Description
7:0	ROA	-	R3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1.



## 8.4.6 Miscellaneous Registers (cont'd)

**Table 166 — Register 0x3E**

R3E			
Bits	Attribute	Default	Description
7:1	RW	001 0100	R3E [7:1]: SWB_DVFSQ_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting for DVFSQ <sup>[1],[2],[3],[4],[5],[6]</sup> 000 0000 = 200 <sup>[7]</sup> mV or 200 <sup>[8]</sup> mV 000 0001 = 205 mV or 202.5 mV 000 0010 = 210 mV or 205 mV ... 001 0100 = 300 mV or 250 mV ... 111 1101 = 825 mV or 512.5 mV 111 1110 = 830 mV or 515 mV 111 1111 = 835 mV or 517.5 mV
0	1O	0	R3E [0]: OUTPUT_VOLTAGE_RESET SWx Output Voltage, Resolution and Offset Reset to Default <sup>[9]</sup> 0 = No action 1 = Reset registers to default <sup>[10],[11]</sup>

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 197, Register 0x4F](#) [7:1].

NOTE 2 If required, the host must update the settings in register [Table 141, Register 0x25](#), [0], [Table 142, Register 0x26](#), [7:2], and [Table 136, Register 0x20](#) [3:2] first prior to updating the settings in the register [Table 166, Register 0x3E](#) [7:1]. Note that SWB DVFSQ threshold settings (Power Good Low Threshold, Power Good High Threshold, Over Voltage Threshold, Under Voltage Threshold) are same regardless of whether PMIC is in P3 or DVFSQ operating state.

NOTE 3 This register is only applicable if [Table 150, Register 0x2E](#)[4] = '1'.

NOTE 4 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 450 mV to 550 mV or from 300 mV to 400 mV depending on the range selection.

NOTE 5 After VR is enabled, the host may update this register to any new setting that it may desire. However, to prevent false error trigger, the PMIC internally will increment the SWB output voltage setting by 5 or 2.5 mV at a time. The time it takes for PMIC to adjust the output voltage is 5  $\mu$ s for each 5 mV increment. The host must wait sufficient time for PMIC to adjust to final value. As an example, if host adjusts the output voltage by 50 mV from the original value, the host must wait minimum of 50  $\mu$ s before PMIC can guarantee the new output voltage. During this time, PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32](#) [5] = '1'.

NOTE 6 The setting in this register must be less than or equal to value programmed in [Table 141, Register 0x25](#), [7:1].

NOTE 7 [Table 147, Register 0x2B](#), [3] = '0'; 5 mV step size.

NOTE 8 [Table 147, Register 0x2B](#), [3] = '1'; 2.5 mV step size.

NOTE 9 This register bit is a self clearing bit.

NOTE 10 The PMIC resets registers [Table 147, Register 0x2B](#), [5:3,0], [Table 137, Register 0x21](#), [7:1], [Table 139, Register 0x23](#), [7:1], [Table 141, Register 0x25](#), [7:1], [Table 143, Register 0x27](#), [7:1], [Table 166, Register 0x3E](#) [7:1], and [Table 167, Register 0x3F](#) [2] to default value.0

NOTE 11 Once this register is written to '1', the PMIC requires time before all registers are reset. During this time, the PMIC masks PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32](#) [5] = '1'.

## 8.4.6 Miscellaneous Registers (cont'd)

**Table 167 — Register 0x3F**

R3F			
Bits	Attribute	Default	Description
7:3	RV	0	R3F [7:3]: Reserved
2	RW	0	R3F [2]: SWB_VOLTAGE_OFFSET SWB Voltage Offset to the setting configured in <a href="#">Table 141, Register 0x25, [7:1]</a> <sup>[1]</sup> 0 = No Offset 1 = 600 mV <sup>[2],[3],[4],[5],[6]</sup> All other encodings are reserved
1:0	RV	0	R3F [1:0]: Reserved

NOTE 1 At first power on, this register is automatically configured identically by PMIC on its own as [Table 206, Register 0x5F \[0\]](#).

NOTE 2 The DVFSQ\_n pin function must be disabled and PMIC cannot be in DVFSQ security state.

NOTE 3 The efficiency spec for SWB does not apply. The DC+AC voltage tolerance for SWB is relaxed to +8% & -5%.

NOTE 4 The SWB output voltage transitions to 600 mV above the value set in [Table 141, Register 0x25, \[7:1\]](#) at a slew rate of 1mV/μs. The 600 mV offset is removed from the value set in [Table 141, Register 0x25, \[7:1\]](#) when this register is cleared to '0' at a slew rate of 1mV/μs.

NOTE 5 It is permitted to change the SWB output voltage.

NOTE 6 The setting in [Table 147, Register 0x2B, \[3\]](#) can be either '0' or '1'.

**Table 168 — Register 0x100**

R100			
Bits	Attribute	Default	Description <sup>[1],[2],[3],[4]</sup>
7:6	RO	-	R100 [7:6]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWA Output Current or Output Power or Total SWA+SWB+SWC+SWD Output Power Measurement <sup>[5]</sup> .  This two MSB bits plus 8 bit register in <a href="#">Table 169, Register 0x102[7:0]</a> makes 10 bit encoding as shown in <a href="#">Table 169, Register 0x102</a> .
5:4	RO	-	R100 [5:4]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWD Output Current or Output Power Measurement.  This two MSB bits plus 8 bit register in <a href="#">Table 170, Register 0x103[7:0]</a> makes 10 bit encoding as shown in <a href="#">Table 170, Register 0x103</a> .
3:2	RO	-	R100 [3:2]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWB Output Current or Output Power Measurement  This two MSB bits plus 8 bit register in <a href="#">Table 171, Register 0x104[7:0]</a> makes 10 bit encoding as shown in <a href="#">Table 171, Register 0x104</a> .
1:0	RO	-	R100 [1:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT_MSB MSB bits - SWC Output Current or Output Power Measurement  This two MSB bits plus 8 bit register in <a href="#">Table 172, Register 0x105[7:0]</a> makes 10 bit encoding as shown in <a href="#">Table 172, Register 0x105</a> .

- NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.
- NOTE 2 This register is only applicable if [Table 154, Register 0x32](#) = '01'.
- NOTE 3 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.
- NOTE 4 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R105) via I<sup>2</sup>C/I<sup>3</sup>C block read commands.
- NOTE 5 The register [Table 131, Register 0x1B](#) [6] must be configured as '1'.

**Table 169 — Register 0x102**

R102			
Bits	Attribute	Default	Description <sup>[1].[2].[3].[4]</sup>
7:0	RO	-	<p>R102 [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB</p> <p>LSB bits - SWA Output Current or Output Power or Total SWA+SWB+SWC+SWD Output Power Measurement</p> <p>The 2 MSB bits <a href="#">Table 168, Register 0x100</a> [7:6] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '0':</p> <p>00 0000 0000 = Undefined</p> <p>00 0000 0001 = 31.25mA or 31.25mW</p> <p>00 0000 0010 = 62.5mA or 62.5mW</p> <p>...</p> <p>11 1111 1111 ≥ 15.936A or 15.936W</p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '1':</p> <p>Sum of SWA, SWD, SWB and SWC Output Power<sup>[5]</sup></p> <p>00 0000 0000 = Undefined</p> <p>00 0000 0001 = 31.25mW</p> <p>00 0000 0010 = 62.5mW</p> <p>...</p> <p>11 1111 1111 ≥ 15.936W</p>

- NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.
- NOTE 2 This register is only applicable if [Table 154, Register 0x32](#) = '01'.
- NOTE 3 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.
- NOTE 4 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R105) via I<sup>2</sup>C/I<sup>3</sup>C block read commands.
- NOTE 5 The register [Table 131, Register 0x1B](#) [6] must be configured as '1'.

## 8.4.6 Miscellaneous Registers (cont'd)

**Table 170 — Register 0x103**

R103			
Bits	Attribute	Default	Description <sup>[1],[2],[3],[4]</sup>
7:0	RO	-	<p>R103 [7:0]: SWD_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWD Output Current or Output Power Measurement</p> <p>The 2 MSB bits <a href="#">Table 168, Register 0x100</a> [5:4] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '0':  00 0000 0000 = Undefined  00 0000 0001 = 31.25 mA or 31.25 mW  00 0000 0010 = 62.5 mA or 62.5 mW  ...  11 1111 1111 <math>\geq</math> 15.936 A or 15.936 W</p>

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 This register is only applicable if [Table 154, Register 0x32](#) = '01'.

NOTE 3 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 4 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R105) via I<sup>2</sup>C/I<sup>3</sup>C block read commands.

**Table 171 — Register 0x104**

R104			
Bits	Attribute	Default	Description <sup>[1],[2],[3],[4]</sup>
7:0	RO	-	<p>R104 [7:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB LSB bits - SWB Output Current or Output Power Measurement</p> <p>The 2 MSB bits <a href="#">Table 168, Register 0x100</a> [3:2] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '0':  00 0000 0000 = Undefined  00 0000 0001 = 31.25 mA or 31.25 mW  00 0000 0010 = 62.5 mA or 62.5 mW  ...  11 1111 1111 <math>\geq</math> 15.936 A or 15.936 W</p>

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 This register is only applicable if [Table 154, Register 0x32](#) = '01'.

NOTE 3 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 4 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R105) via I<sup>2</sup>C/I<sup>3</sup>C block read commands.

## 8.4.6 Miscellaneous Registers (cont'd)

**Table 172 — Register 0x105**

R105			
Bits	Attribute	Default	Description <sup>[1],[2],[3],[4]</sup>
7:0	RO	-	<p>R105 [7:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT_LSB</p> <p>LSB bits - SWC Output Current or Output Power Measurement</p> <p>The 2 MSB bits <a href="#">Table 168, Register 0x100</a> [1:0] plus this 8 bit register makes 10 bit encoding as shown below.</p> <p>If <a href="#">Table 130, Register 0x1A</a>[1] = '0':</p> <p>00 0000 0000 = Undefined</p> <p>00 0000 0001 = 31.25 mA or 31.25 mW</p> <p>00 0000 0010 = 62.5 mA or 62.5 mW</p> <p>...</p> <p>11 1111 1111 <math>\geq</math> 15.936 A or 15.936 W</p>

NOTE 1 The PMIC reports current or power measurement as long as there is no output over voltage or output under voltage lockout event that triggers the VR Disable command. If PMIC triggers VR Disable command, PMIC does not report current or power measurement and register content may have stale data. For all other events that causes PMIC's power good status as Not Good, the PMIC continues to provide current or power measurement.

NOTE 2 This register is only applicable if [Table 154, Register 0x32](#) = '01'.

NOTE 3 If [Table 131, Register 0x1B](#) [6] = '0', the PMIC reports current measurement. If [Table 131, Register 0x1B](#) [6] = '1', the PMIC reports power measurement.

NOTE 4 The Host must read ADC current or power measurement bytes in order from MSB to LSB (i.e., R100 to R105) via I<sup>2</sup>C/I<sup>3</sup>C block read commands.

**Table 173 — Register 0x109**

R109			
Bits	Attribute	Default	Description
7:1	RV	-	R109 [7:1]: Reserved
0	RO	-	<p>R109 [0]: SWB_DISABLE_PIN_INPUT_STATUS_AT_VR_EN</p> <p>SWB_Disable Input Pin Level Status at VR_EN Command<sup>[1],[2],[3]</sup></p> <p>0 = Low</p> <p>1 = High</p>

NOTE 1 The controller cannot clear this register via any I<sup>2</sup>C/I<sup>3</sup>C bus command.

NOTE 2 The PMIC clears this register when PMIC executes VR Disable command (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or PWR\_GOOD input or fault event)

NOTE 3 At first power on, prior to first VR Enable command, the default register value is a don't care.

**Table 174 — Register 0x130**

R130			
Bits	Attribute	Default	Description
7:0	ROA	-	<p>R130 [7:0]: SERIAL_NUMBER_BYTE_0</p> <p>Byte 0 of the unique 40-bit serial number</p> <p>Serial number is vendor specific</p>

**8.4.6 Miscellaneous Registers (cont'd)****Table 175 — Register 0x131**

R131			
Bits	Attribute	Default	Description
7:0	ROA	-	R131 [7:0]: SERIAL_NUMBER_BYTE_1 Byte 1 of the unique 40-bit serial number Serial number is vendor specific

**Table 176 — Register 0x132**

R132			
Bits	Attribute	Default	Description
7:0	ROA	-	R132 [7:0]: SERIAL_NUMBER_BYTE_2 Byte 2 of the unique 40-bit serial number Serial number is vendor specific

**Table 177 — Register 0x133**

R133			
Bits	Attribute	Default	Description
7:0	ROA	-	R133 [7:0]: SERIAL_NUMBER_BYTE_3 Byte 3 of the unique 40-bit serial number Serial number is vendor specific

**Table 178 — Register 0x134**

R134			
Bits	Attribute	Default	Description
7:0	ROA	-	R134 [7:0]: SERIAL_NUMBER_BYTE_4 Byte 4 of the unique 40-bit serial number Serial number is vendor specific

**Table 179 — Register 0x135**

R135			
Bits	Attribute	Default	Description
7:0	ROA	-	R135 [7:0]: SERIAL_NUMBER_BYTE_5 Byte 5 of the unique 40-bit serial number Serial number is vendor specific

**Table 180 — Register 0x136**

R136			
Bits	Attribute	Default	Description
7:0	ROA	-	R136 [7:0]: SERIAL_NUMBER_BYTE_6 Byte 6 of the unique 40-bit serial number Serial number is vendor specific

## 8.5 CAMM2 Vendor Region Register Definition

**Table 181 — CAMM2 Vendor Region - Register Map**

Register	Attribute	Description
Table 182, Register 0x40	RWPE	R40 [7:0] Power On Sequence - Configuration 0
Table 183, Register 0x41	RWPE	R41 [7:0] Power On Sequence - Configuration 1
Table 184, Register 0x42	RWPE	R42 [7:0] Power On Sequence - Configuration 2
Table 185, Register 0x43	RWPE	R43 [7:0] Power On Sequence - Configuration 3
Table 186, Register 0x44	RWPE	R44 [7:4] Soft Stop Time Extension R44 [3:1] Reserved R44 [0] SWB_Disable Input Pin Enable
Table 187, Register 0x45	RWPE	R45 [7:1] SWA Voltage Setting R45 [0] SWA Power Good Low Side Threshold
Table 188, Register 0x46	RWPE	R46 [7:6] SWA Power Good High Side Threshold R46 [5:4] SWA Over Voltage Threshold R46 [3:2] SWA Under Voltage Lockout Threshold R46 [1:0] SWA Soft Stop Time
Table 189, Register 0x47	RWPE	R47 [7:1] SWD Voltage Setting R47 [0] SWD Power Good Low Side Threshold
Table 190, Register 0x48	RWPE	R48 [7:6] SWD Power Good High Side Threshold R48 [5:4] SWD Over Voltage Threshold R48 [3:2] SWD Under Voltage Lockout Threshold R48 [1:0] SWD Soft Stop Time
Table 191, Register 0x49	RWPE	R49 [7:1] SWB Voltage Setting R49 [0] SWB Power Good Low Side Threshold
Table 192, Register 0x4A	RWPE	R4A [7:6] SWB Power Good High Side Threshold R4A [5:4] SWB Over Voltage Threshold R4A [3:2] SWB Under Voltage Lockout Threshold R4A [1:0] SWB Soft Stop Time
Table 193, Register 0x4B	RWPE	R4B [7:1] SWC Voltage Setting R4B [0] SWC Power Good Low Side Threshold
Table 194, Register 0x4C	RWPE	R4C [7:6] SWC Power Good High Side Threshold R4C [5:4] SWC Over Voltage Threshold R4C [3:2] SWC Under Voltage Lockout Threshold R4C [1:0] SWC Soft Stop Time
Table 195, Register 0x4D	RWPE	R4D [7:6] SWA Mode Select R4D [5:4] SWA Switching Frequency R4D [3:2] SWD Mode Select R4D [1:0] SWD Switching Frequency
Table 196, Register 0x4E	RWPE	R4E [7:6] SWB Mode Select R4E [5:4] SWB Switching Frequency R4E [3:2] SWC Mode Select R4E [1:0] SWC Switching Frequency
Table 197, Register 0x4F	RWPE	R4F [7:1] SWB_DVFSQ_VOLTAGE_SETTING R4F [0] Reserved

**Table 181 — CAMM2 Vendor Region - Register Map (cont'd)**

Register	Attribute	Description
Table 198, Register 0x50	RWPE	R50 [7:6] SWA Output Current Limiter Warning Threshold R50 [5:4] SWD Output Current Limiter Warning Threshold R50 [3:2] SWB Output Current Limiter Warning Threshold R50 [1:0] SWC Output Current Limiter Warning Threshold
Table 199, Register 0x51	RWPE	R51 [7:6] VOUT_1.8V LDO Output Voltage Setting R51 [5:3] SWA, SWD, SWB Output Voltage Step Size Resolution R51 [2:1] VOUT_1.0V LDO Voltage Setting R51 [0] SWC Output Voltage Step Size Resolution
0x52 - 0x57	RV	R52 [7:0] - R57 [7:0] Reserved
Table 200, Register 0x58	RWPE	R58 [7:0] Power Off Sequence - Configuration 0
Table 201, Register 0x59	RWPE	R59 [7:0] Power Off Sequence - Configuration 1
Table 202, Register 0x5A	RWPE	R5A [7:0] Power Off Sequence - Configuration 2
Table 203, Register 0x5B	RWPE	R5B [7:0] Power Off Sequence - Configuration 3
0x5C	RV	R5C [7:0] Reserved
Table 204, Register 0x5D	RWPE	R5D [7:5] SWA Soft Start Time R5D [4] Reserved R5D [3:1] SWD Soft Start Time R5D [0] Reserved
Table 205, Register 0x5E	RWPE	R5E [7:5] SWB Soft Start Time R5E [4] Reserved R5E [3:1] SWC Soft Start Time R5E [0] Reserved
Table 206, Register 0x5F	RWPE	R5F [7] Host Region R2F[2] Register Control R5F [6] PMIC Auto Power On Control R5F [5:4] Reserved R5F [3] Unlock input pin enable R5F [2:1] SWB DVFSQ Voltage Slew Rate R5F [0] SWB Voltage Offset
0x60 to 0x66	RV	R60 [7:0] to R66 [7:0] Reserved
Table 207, Register 0x67	RWPE	R67 [7:0] SWA Output High Current Consumption Warning Threshold
Table 208, Register 0x68	RWPE	R68 [7:0] SWD Output High Current Consumption Warning Threshold
Table 209, Register 0x69	RWPE	R69 [7:0] SWB Output High Current Consumption Warning Threshold
Table 210, Register 0x6A	RWPE	R6A [7:0] SWC Output High Current Consumption Warning Threshold
0x6B to 0x6C	RV	R6B [7:0] to R6C [7:0] Reserved
Table 211, Register 0x6D	RWPE	R6D [7:5] SWA Max Vout Detection Threshold R6D [4] SWA Unsupported Voltage Detection Status R6D [3:1] SWD Max Vout Detection Threshold R6D [0] SWD Unsupported Voltage Detection Status
Table 212, Register 0x6E	RWPE	R6E [7:5] SWB Max Vout Detection Threshold R6E [4] SWB Unsupported Voltage Detection Status R6E [3] Reserved R6E [2:1] SWC Max Vout Detection Threshold R6E [0] SWC Unsupported Voltage Detection Status
0x6F	RV	R6F [7:0] Reserved



## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 182 — Register 0x40<sup>[1]</sup>**

R40			
Bits	Attribute	Default	Description
7	RWPE	0	R40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power On Sequence Config 0 <sup>[2]</sup> 0 = Do Not Execute Config 0 1 = Execute Config 0
6	RWPE	0	R40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No action 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R40 [5]: POWER_ON_SEQUENCE_CONFIG0_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No action 1 = Enable Switch Node D Output Regulator
4	RWPE	0	R40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator <sup>[3]</sup> 0 = No action 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No action 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power On Sequence Config 0 <sup>[4]</sup> 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms

NOTE 1 The PMIC always starts with power on sequence config0 and executes remaining power on sequence config registers (1 to 3) in sequential order.

NOTE 2 If bit [7] = '0', bits [6:0] are ignored and PMIC moves to next power on sequence configuration register. If bits [7] = '1', the PMIC executes bits [6:0] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 3 The SWB output regulator is conditionally enabled as defined in clause 4.13. The SWB output rail remains disabled even if this is bit set to '1', if SWB\_Disable input pin is enabled, and its input level is either high at the time of VR Enable command (either from VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on) from P2\_B state.

NOTE 4 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 183 — Register 0x41<sup>[1]</sup>**

R41			
Bits	Attribute	Default	Description
7	RWPE	0	R41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power On Sequence Config 1 0 = Do Not Execute Config 1 <sup>[2]</sup> 1 = Execute Config 1
6	RWPE	0	R41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No action 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R41 [5]: POWER_ON_SEQUENCE_CONFIG1_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No action 1 = Enable Switch Node D Output Regulator
4	RWPE	0	R41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator <sup>[3]</sup> 0 = No action 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No action 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power On Sequence Config 1 <sup>[4]</sup> 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms

NOTE 1 The PMIC always starts with power on sequence config0 and executes remaining power on sequence config registers (1 to 3) in sequential order.

NOTE 2 If bit [7] = '0', bits [6:0] are ignored and PMIC moves to next power on sequence configuration register. If bits [7] = '1', the PMIC executes bits [6:0] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 3 The SWB output regulator is conditionally enabled as defined in clause 4.13. The SWB output rail remains disabled even if this is bit set to '1', if SWB\_Disable input pin is enabled, and its input level is either high at the time of VR Enable command (either from VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on) from P2\_B state.

NOTE 4 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 184 — Register 0x42<sup>[1],[2]</sup>**

R42			
Bits	Attribute	Default	Description
7	RWPE	0	R42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power On Sequence Config 2 <sup>[3]</sup> 0 = Do Not Execute Config 2 1 = Execute Config 2
6	RWPE	0	R42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No action 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R42 [5]: POWER_ON_SEQUENCE_CONFIG2_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No action 1 = Enable Switch Node D Output Regulator
4	RWPE	0	R42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator <sup>[4]</sup> 0 = No action 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No action 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power On Sequence Config 2 <sup>[5]</sup> 000 = 0 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms 100 = 8 ms 101 = 10 ms 110 = 12 ms 111 = 24 ms

NOTE 1 The PMIC always starts with power on sequence config0 and executes remaining power on sequence config registers (1 to 3) in sequential order

NOTE 2 If more than one configuration register is used for power on sequence, first register must start at [Table 182, Register 0x40](#) and it must go in sequential order to [Table 185, Register 0x43](#) to turn on all desired regulators. In other words, there must not be any gap of the register that is used for power on sequence.

NOTE 3 If bit [7] = '0', bits [6:0] are ignored and PMIC moves to next power on sequence configuration register. If bits [7] = '1', the PMIC executes bits [6:0] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 4 The SWB output regulator is conditionally enabled as defined in clause 4.13. The SWB output rail remains disabled even if this is bit set to '1', if SWB\_Disable input pin is enabled, and its input level is either high at the time of VR Enable command (either from VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on) from P2\_B state.

NOTE 5 Idle time is the additional time after soft-start time expires. The PMIC waits sum of Soft Start time and Idle time before it executes the next power on sequence configuration register. If more than one regulators are enabled, the PMIC uses the largest value of the soft start time among the regulators that are enabled in this configuration register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 185 — Register 0x43<sup>[1]</sup>**

R43			
Bits	Attribute	Default	Description
7	RWPE	0	R43 [7]: POWER_ON_SEQUENCE_CONFIG3 PMIC Power On Sequence Config 3 <sup>[2]</sup> 0 = Do Not Execute Config 3 1 = Execute Config 3
6	RWPE	0	R43 [6]: POWER_ON_SEQUENCE_CONFIG3_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = No action 1 = Enable Switch Node A Output Regulator
5	RWPE	0	R43 [5]: POWER_ON_SEQUENCE_CONFIG3_SWD_ENABLE Enable Switch Node D Output Regulator. 0 = No action 1 = Enable Switch Node D Output Regulator
4	RWPE	0	R43 [4]: POWER_ON_SEQUENCE_CONFIG3_SWB_ENABLE Enable Switch Node B Output Regulator. <sup>[3]</sup> 0 = No action 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R43 [3]: POWER_ON_SEQUENCE_CONFIG3_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = No action 1 = Enable Switch Node C Output Regulator
2:0	RV	0	R43 [2:0]: Reserved

NOTE 1 The PMIC always starts with power on sequence config0 and executes remaining power on sequence config registers (1 to 3) in sequential order.

NOTE 2 If bit [7] = '0', bits [6:0] are ignored and PMIC moves to next power on sequence configuration register. If bits [7] = '1', the PMIC executes bits [6:0] as configured; if no new rail is turned on, the PMIC simply waits the idle time as configured and then moves to next power sequence configuration register.

NOTE 3 The SWB output regulator is conditionally enabled as defined in clause 4.13. The SWB output rail remains disabled even if this is bit set to '1', if SWB\_Disable input pin is enabled, and its input level is either high at the time of VR Enable command (either from VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on) from P2\_B state.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 186 — Register 0x44**

R44			
Bits	Attribute	Default	Description
7	RWPE	0	R44 [7]: SWA_OUTPUT_SOFT_STOP_TIME_EXTENSION SWA Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 188, Register 0x46</a> [1:0] makes 3 bit register encoding. See encoding in <a href="#">Table 188, Register 0x46</a> .
6	RWPE	0	R44 [6]: SWD_OUTPUT_SOFT_STOP_TIME_EXTENSION SWD Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 190, Register 0x48</a> [1:0] makes 3 bit register encoding. See encoding in <a href="#">Table 190, Register 0x48</a> .
5	RWPE	0	R44 [5]: SWB_OUTPUT_SOFT_STOP_TIME_EXTENSION SWB Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 192, Register 0x4A</a> [1:0] makes 3 bit register encoding. See encoding in <a href="#">Table 192, Register 0x4A</a> .
4	RWPE	0	R44 [4]: SWC_OUTPUT_SOFT_STOP_TIME_EXTENSION SWC Output Regulator Soft Stop Time After VR Disable. This register bit (MSB) plus 2 bit register <a href="#">Table 194, Register 0x4C</a> [1:0] makes 3 bit register encoding. See encoding in <a href="#">Table 194, Register 0x4C</a> .
3:1	RV	0	R44 [3:1]: Reserved
0	RWPE	1	R44 [0]: SWB_DISABLE_INPUT_PIN_ENABLE SWB_Disable Input Pin Enable 0 = Disable; Input pin receiver is disabled 1 = Enable; Input pin receiver is enabled

**Table 187 — Register 0x45**

R45			
Bits	Attribute	Default	Description
7:1	RWPE	011 0010	R45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting <sup>[1]</sup> 000 0000 = 800 <sup>[2]</sup> mV or 800 <sup>[3]</sup> mV 000 0001 = 805 mV or 810 mV 000 0010 = 810 mV or 820 mV ... 011 1100 = 1100 mV or 1400 mV ... 111 1101 = 1425 mV or 2050 mV 111 1110 = 1430 mV or 2060 mV 111 1111 = 1435 mV or 2070 mV
0	RWPE	0	R45 [1:0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low Side Voltage For Power Good Status 0 = - 5% from the setting in <a href="#">Table 187, Register 0x45</a> [7:1] 1 = - 7.5% from the setting in <a href="#">Table 187, Register 0x45</a> [7:1]

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1000 mV to 1100 mV.

NOTE 2 [Table 199, Register 0x51](#) [5] = '0'; 5 mV step size.

NOTE 3 [Table 199, Register 0x51](#) [5] = '1'; 10 mV step size.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

Table 188 — Register 0x46

R46			
Bits	Attribute	Default	Description
7:6	RWPE	01	R46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 01 = +7.5% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 10 = +10% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 11 = Reserved
5:4	RWPE	10	R46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over Voltage Status <sup>[1]</sup> 00 = +7.5% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 01 = +10% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 10 = +12.5% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 11 = Reserved
3:2	RWPE	00	R46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 01 = -12.5% from the setting in <a href="#">Table 187, Register 0x45 [7:1]</a> 10 = Reserved 11 = Reserved
1:0	RWPE	00	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft Stop Time After VR Disable <sup>[2]</sup> . The register <a href="#">Table 186, Register 0x44 [7]</a> (MSB) plus this two bit register makes the 3 bit encoding. 000 = 0.5 ms 001 = 1 ms 010 = 2 ms 011 = 4 ms 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 188, Register 0x46\[7:6\]](#).

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 189 — Register 0x47**

R47			
Bits	Attribute	Default	Description
7:1	RWPE	001 0100	R47 [7:1]: SWD_VOLTAGE_SETTING Switch Node D Output Regulator Voltage Setting <sup>[1]</sup> 000 0000 = 800 <sup>[2]</sup> mV or 800 <sup>[3]</sup> mV 000 0001 = 805 mV or 810 mV 000 0010 = 810 mV or 820 mV ... 011 1100 = 1100 mV or 1400 mV ... 111 1101 = 1425 mV or 2050 mV 111 1110 = 1430 mV or 2060 mV 111 1111 = 1435 mV or 2070 mV
0	RWPE	0	R47 [1:0]: SWD_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold Low Side Voltage For Power Good Status 0 = - 5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 1 = - 7.5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1]

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 850 mV to 950 mV.

NOTE 2 [Table 199, Register 0x51](#) [4] = '0'; 5 mV step size.

NOTE 3 [Table 199, Register 0x51](#) [4] = '1'; 10 mV step size.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 190 — Register 0x48**

R48			
Bits	Attribute	Default	Description
7:6	RWPE	01	R48 [7:6]: SWD_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node D Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 01 = +7.5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 10 = +10% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 11 = Reserved
5:4	RWPE	10	R48 [5:4]: SWD_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Over Voltage Status <sup>[1]</sup> 00 = +7.5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 01 = +10% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 10 = +12.5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 11 = Reserved
3:2	RWPE	00	R48 [3:2]: SWD_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node D Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 01 = -12.5% from the setting in <a href="#">Table 189, Register 0x47</a> [7:1] 10 = Reserved 11 = Reserved
1:0	RWPE	00	R48 [1:0]: SWD_OUTPUT_SOFT_STOP_TIME SWD Output Regulator Soft Stop Time After VR Disable <sup>[2]</sup> . The register <a href="#">Table 186, Register 0x44</a> [6] (MSB) plus this two bit register makes the 3 bit encoding. 000 = 0.5 ms 001 = 1 ms 010 = 2 ms 011 = 4 ms 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 190, Register 0x48](#) [7:6].

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.



## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 191 — Register 0x49**

R49			
Bits	Attribute	Default	Description
7:1	RWPE	011 1100	R49 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting <sup>[1]</sup> 000 0000 = 200 <sup>[2]</sup> mV or 200 <sup>[3]</sup> mV 000 0001 = 205 mV or 202.5 mV 000 0010 = 210 mV or 205 mV ... 011 1100 = 500 mV or 350 mV ... 111 1101 = 825 mV or 512.5 mV 111 1110 = 830 mV or 515 mV 111 1111 = 835 mV or 517.5 mV
0	RWPE	0	R49 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in <a href="#">Table 191, Register 0x49 [7:1]</a> 1 = -7.5 from the setting in <a href="#">Table 191, Register 0x49 [7:1]</a>

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 450 mV to 550 mV or from 300 mV to 400 mV depending on the range selection.

NOTE 2 [Table 199, Register 0x51 \[3\]](#) = '0'; 5 mV step size.

NOTE 3 [Table 199, Register 0x51 \[3\]](#) = '1'; 2.5 mV step size.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 192 — Register 0x4A**

R4A			
Bits	Attribute	Default	Description
7:6	RWPE	01	R4A [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 01 = +7.5% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 10 = +10% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 11 = Reserved
5:4	RWPE	10	R4A [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over Voltage Status <sup>[1]</sup> 00 = +7.5% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 01 = +10% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 10 = +12.5% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 11 = Reserved
3:2	RWPE	00	R4A [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 01 = -12.5% from the setting in <a href="#">Table 191, Register 0x49</a> [7:1] 10 = Reserved 11 = Reserved
1:0	RWPE	00	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft Stop Time After VR Disable <sup>[2]</sup> . The register <a href="#">Table 186, Register 0x44</a> [5] (MSB) plus this two bit register makes the 3 bit encoding. 000 = 0.5 ms 001 = 1 ms 010 = 2 ms 011 = 4 ms 100 = 8 ms 101 = 16 ms 110 = 32 ms 111 = 64 ms

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 192, Register 0x4A](#)[7:6].

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

Table 193 — Register 0x4B

R4B			
Bits	Attribute	Default	Description
7:1	RWPE	011 1100	R4B [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting <sup>[1]</sup> 000 0000 = 1500 <sup>[2]</sup> mV or 1500 <sup>[3]</sup> mV 000 0001 = 1505 mV or 1510 mV 000 0010 = 1510 mV or 1520 mV ... 011 1100 = 1800 mV or 2100 mV ... 111 1101 = 2125 mV or 2750 mV 111 1110 = 2130 mV or 2760 mV 111 1111 = 2135 mV or 2770 mV
0	RWPE	0	R4B [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low Side Voltage For Power Good Status 0 = -5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 1 = -7.5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a>

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 1750 mV to 1850 mV.

NOTE 2 [Table 199, Register 0x51 \[0\]](#) = '0'; 5 mV step size.

NOTE 3 [Table 199, Register 0x51 \[0\]](#) = '0'; 10 mV step size.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 194 — Register 0x4C**

R4C			
Bits	Attribute	Default	Description
7:6	RWPE	01	R4C [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High Side Voltage For Power Good Status 00 = +5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 01 = +7.5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 10 = +10% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 11 = Reserved
5:4	RWPE	10	R4C [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over Voltage Status <sup>[1]</sup> 00 = +7.5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 01 = +10% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 10 = +12.5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 11 = Reserved
3:2	RWPE	00	R4C [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under Voltage Lockout Status 00 = -10% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 01 = -12.5% from the setting in <a href="#">Table 193, Register 0x4B [7:1]</a> 10 = Reserved 11 = Reserved
1:0	RWPE	00	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft Stop Time After VR Disable <sup>[2]</sup> . The register <a href="#">Table 186, Register 0x44 [4]</a> (MSB) plus this two bit register makes the 3 bit encoding. 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 8 ms 100 = 16 ms 101 = 32 ms 110 = 64 ms 111 = Vendor defined

NOTE 1 The setting for the Over Voltage must be higher than Power Good High Side Voltage threshold in [Table 194, Register 0x4C\[7:6\]](#).

NOTE 2 This is the time it takes for buck regulator to go from steady state voltage to 0 V.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 195 — Register 0x4D**

R4D			
Bits	Attribute	Default	Description
7:6	RWPE	10	R4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = 500 KHz
3:2	RWPE	10	R4D [3:2]: SWD_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	R4D [1:0]: SWD_SWITCHING_FREQ Switch Node D Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = Vendor specific

**8.5 CAMM2 Vendor Region Register Definition (cont'd)****Table 196 — Register 0x4E**

R4E			
Bits	Attribute	Default	Description
7:6	RWPE	10	R4E [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4E [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = Vendor specific
3:2	RWPE	10	R4E [3:2]: SWC_MODE_SELECT Switch Node C Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	R4E [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750 KHz 01 = Vendor specific 10 = Vendor specific 11 = Vendor specific

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 197 — Register 0x4F**

R4F			
Bits	Attribute	Default	Description
7:1	RWPE	001 0100	R4F [7:1]: SWB_DVFSQ_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting for DVFSQ <sup>[1],[2]</sup> 000 0000 = 200 <sup>[3]</sup> mV or 200 <sup>[4]</sup> mV 000 0001 = 205 mV or 202.5 mV 000 0010 = 210 mV or 205 mV ... 001 0100 = 300 mV or 250 mV ... 111 1101 = 825 mV or 512.5 mV 111 1110 = 830 mV or 515 mV 111 1111 = 835 mV or 517.5 mV
0	RV	0	R4F [0]: Reserved

NOTE 1 PMIC guarantees efficiency spec and all electrical characteristics spec within a range of 450 mV to 550 mV or from 300 mV to 400 mV, depending on the range selection.

NOTE 2 The setting in this register must be less than or equal to value programmed in [Table 191, Register 0x49](#) [7:1].

NOTE 3 [Table 199, Register 0x51](#) [3] = '0'; 5 mV step size.

NOTE 4 [Table 199, Register 0x51](#) [3] = '1'; 2.5 mV step size.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 198 — Register 0x50**

R50			
Bits	Attribute	Default	Description
7:6	RWPE	0	R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node A Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 7.5. A 01 = 8.5 A 10 = 9.5. A 11 = Vendor specific
5:4	RWPE	0	R50 [5:4]: SWD_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node D Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 0.5 A 01 = 1.0 A 10 = 1.5 A 11 = Vendor specific
3:2	RWPE	0	R50 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node B Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 0.5 A 01 = 1.0 A 10 = 1.5 A 11 = Vendor specific
1:0	RWPE	0	R50 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node C Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 0.5 A 01 = 1.0 A 10 = Reserved 11 = Vendor specific



## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 199 — Register 0x51**

R51			
Bits	Attribute	Default	Description
7:6	RWPE	01	R51 [7:6]: VOUT_1.8V_VOLTAGE_SETTING VOUT 1.8 V LDO Output Voltage Setting <sup>[1]</sup> 00 = 1.7 V 01 = 1.8 V 10 = 1.9 V 11 = 2.0 V
5	RWPE	0	R51 [5]: SWA_VOLTAGE_STEP_SIZE SWA Voltage Step Size 0 = 5 mV 1 = 10 mV
4	RWPE	0	R51 [4]: SWD_VOLTAGE_STEP_SIZE SWD Voltage Step Size 0 = 5 mV 1 = 10 mV
3	RWPE	0	R51 [3]: SWB_VOLTAGE_STEP_SIZE SWB Output Voltage Range Selection 0 = 5 mV 1 = 2.5 mV
2:1	RWPE	01	R51 [2:1]: VOUT_1.0V_VOLTAGE_SETTING VOUT 1.0 V LDO Voltage Setting 00 = 0.9 V 01 = 1.0 V 10 = 1.1 V 11 = 1.2 V
0	RWPE	0	R51 [0]: SWC_VOLTAGE_STEP_SIZE SWC Voltage Step Size 0 = 5 mV 1 = 10 mV

NOTE 1 The VOUT\_1.8V Power Good threshold in register [Table 130, Register 0x1A](#) [2] is always fixed, regardless of the setting in this register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 200 — Register 0x58<sup>[1]</sup>**

R58			
Bits	Attribute	Default	Description
7	RWPE	0	R58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power Off Sequence Config 0 0 = Do Not Execute Config 0 <sup>[2]</sup> 1 = Execute Config 0
6	RWPE	0	R58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = No action 1 = Disable Switch Node A Output Regulator
5	RWPE	0	R58 [5]: POWER_OFF_SEQUENCE_CONFIG0_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No action 1 = Disable Switch Node D Output Regulator
4	RWPE	0	R58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Disable Switch Node B Output Regulator 0 = No action 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No action 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power Off Sequence Config 0 <sup>[3]</sup> 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms

NOTE 1 If more than one configuration register is used for power off sequence, first register must start at [Table 200, Register 0x58](#) and it must go in sequential order to [Table 203, Register 0x5B](#) to turn off all regulators. In other words, there must not be any gap of the register that is used for power off sequence.

NOTE 2 If bit [7] = '0', bits [6:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6:3] must be programmed as '1'.

NOTE 3 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 201 — Register 0x59<sup>[1],[2]</sup>**

R59			
Bits	Attribute	Default	Description
7	RWPE	0	R59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power Off Sequence Config1 <sup>[3]</sup> 0 = Do Not Execute Config 1 1 = Execute Config 1
6	RWPE	0	R59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = No action 1 = Disable Switch Node A Output Regulator
5	RWPE	0	R59 [5]: POWER_OFF_SEQUENCE_CONFIG1_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No action 1 = Disable Switch Node D Output Regulator
4	RWPE	0	R59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Disable Switch Node B Output Regulator 0 = No action 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No action 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power Off Sequence Config 1 <sup>[4]</sup> 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms

NOTE 1 If any regulators are disabled in [Table 200, Register 0x58](#) [6:3], those regulators must be configured as '1' in this sequence.

NOTE 2 If more than one configuration register is used for power off sequence, first register must start at [Table 200, Register 0x58](#) and it must go in sequential order to [Table 203, Register 0x5B](#) to turn off all regulators. In other words, there must not be any gap of the register that is used for power off sequence.

NOTE 3 If bit [7] = '0', bits [6:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6:3] must be programmed as '1'.

NOTE 4 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 202 — Register 0x5A<sup>[1],[2]</sup>**

R5A			
Bits	Attribute	Default	Description
7	RWPE	0	R5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power Off Sequence Config 2 <sup>[3]</sup> 0 = Do Not Execute Config 2 1 = Execute Config 2
6	RWPE	0	R5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = No action 1 = Disable Switch Node A Output Regulator
5	RWPE	0	R5A [5]: POWER_OFF_SEQUENCE_CONFIG2_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No action 1 = Disable Switch Node D Output Regulator
4	RWPE	0	R5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Disable Switch Node B Output Regulator 0 = No action 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No action 1 = Disable Switch Node C Output Regulator
2:0	RWPE	0	R5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power Off Sequence Config 2 <sup>[4]</sup> 000 = 0 ms 001 = 1 ms 010 = 2 ms 011 = 3 ms 100 = 4 ms 101 = 5 ms 110 = 6 ms 111 = 7 ms

NOTE 1 If any regulators are disabled in [Table 200, Register 0x58](#) [6:3] and [Table 201, Register 0x59](#), [6:3], those regulators must be configured as '1' in this sequence.

NOTE 2 If more than one configuration register is used for power off sequence, first register must start at [Table 200, Register 0x58](#) and it must go in sequential order to [Table 203, Register 0x5B](#) to turn off all regulators. In other words, there must not be any gap of the register that is used for power off sequence.

NOTE 3 If bit [7] = '0', bits [6:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6:3] must be programmed as '1'.

NOTE 4 Idle time is the additional time after soft-stop time expires. The PMIC waits sum of soft stop time and idle time before it executes the next power off sequence configuration register. If more than one regulators are disabled, the PMIC uses the largest value of the soft stop time among the regulators that are disabled in this configuration register.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 203 — Register 0x5B<sup>[1]</sup>**

R5B			
Bits	Attribute	Default	Description
7	RWPE	0	R5B [7]: POWER_OFF_SEQUENCE_CONFIG3 PMIC Power Off Sequence Config 3 <sup>[2]</sup> 0 = Do Not Execute Config 3 1 = Execute Config 3
6	RWPE	0	R5B [6]: POWER_OFF_SEQUENCE_CONFIG3_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = No action 1 = Disable Switch Node A Output Regulator
5	RWPE	0	R5B [5]: POWER_OFF_SEQUENCE_CONFIG3_SWD_DISABLE Disable Switch Node D Output Regulator. 0 = No action 1 = Disable Switch Node D Output Regulator
4	RWPE	0	R5B [4]: POWER_OFF_SEQUENCE_CONFIG3_SWB_DISABLE Disable Switch Node B Output Regulator 0 = No action 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R5B [3]: POWER_OFF_SEQUENCE_CONFIG3_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = No action 1 = Disable Switch Node C Output Regulator
2:0	RV	0	R5B [2:0]: Reserved

NOTE 1 If any regulators are disabled in [Table 200, Register 0x58](#) [6:3], [Table 201, Register 0x59](#), [6:3], and [Table 202, Register 0x5A](#), [6:3], those regulators must be configured as '1' in this sequence.

NOTE 2 If bit [7] = '0', bits [6:3] must be programmed as '000'. If bit [7] = '1', at least one of the bits [6:3] must be programmed as '1'.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 204 — Register 0x5D**

R5D			
Bits	Attribute	Default	Description
7:5	RWPE	001	R5D [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft Start Time After VR Enable <sup>[1]</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4	RV	0	R5D [4]: Reserved
3:1	RWPE	001	R5D [3:1]: SWD_OUTPUT_SOFT_START_TIME SWD Output Regulator Soft Start Time After VR Enable <sup>[2]</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
0	RWPE	0	R5D [0]: Reserved

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

NOTE 2 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage).

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 205 — Register 0x5E**

R5E			
Bits	Attribute	Default	Description
7:5	RWPE	001	R5E [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft Start Time After VR Enable <sup>[1]</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
4	RV	0	R5E [4]: Reserved
3:1	RWPE	001	R5E [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft Start Time After VR Enable <sup>1</sup> 000 = 1 ms 001 = 2 ms 010 = 4 ms 011 = 6 ms ... 111 = 14 ms
0	RV	0	R5E [0]: Reserved

NOTE 1 This is the time it takes for buck regulator to go from 0 V to steady state voltage (the actual voltage varies based on pre-programmed voltage)

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

Table 206 — Register 0x5F

R5F			
Bits	Attribute	Default	Description
7	RWPE	0	R5F [7]: R2F_CONTROL Host Region R2F[2] Register Setting at First Power On 0 = R2F [2] = 0 1 = R2F [2] = 1
6	RWPE	0	R5F [6]: PMIC_AUTO_POWER_ON PMIC Auto Power On Control 0 = PMIC requires VR_EN pin assertion or VR_EN command (i.e., R32 [7] = 1) to turn on output rails 1 = PMIC automatically executes R32 [7] = 1 as soon as it detects valid VIN_Bulk and turns on output rails.
5:4	RV	0	R5F [5:4]: Reserved
3	RWPE	1	R5F [3]: UNLOCK_INPUT_PIN_ENABLE Unlock Input Pin Enable 0 = Disable; Unlock input pin receiver is disabled 1 = Enable; Unlock input pin receiver is enabled
2:1	RWPE	11	R5F [2:1]: SWB_DVFSQ_VOLTAGE_SLEW_RATE SWB Output Voltage Slew Rate when transitioning from P3 to DVFSQ and DVFSQ to P3 state <sup>[1]</sup> 00 = 15 mV/μs 01 = 10 mV/μs 10 = 5 mV/μs 11 = 1 mV/μs
0	RWPE	0	R5F [0]: SWB_VOLTAGE_OFFSET SWB Voltage Offset to the setting configured in <a href="#">Table 191, Register 0x49</a> [7:1] 0 = No Offset 1 = 600 mV Offset

NOTE 1 During the SWB output voltage transition, the PMIC masks the PWR\_GOOD output signal assertion to prevent any artificial error due to the crossing of the output voltage threshold setting and keeps the PWR\_GOOD signal Hi-Z. However, PMIC does assert PWR\_GOOD output signal if there are any abnormal issues that triggers VR Disable command as described in [Table 27](#). Further, PMIC does monitor PWR\_GOOD input signal and executes power off config sequence registers if it is registered low when [Table 154, Register 0x32](#) [5] = '1'.



## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 207 — Register 0x67**

R67			
Bits	Attribute	Default	Description
7:0	RW	1111 0000	<p>R67 [7:0]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold</p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '00':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 125 mA            0000 0010 <math>\geq</math> 250 mA            ...            1111 1111 <math>\geq</math> 31.875A</p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '01':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 31.25 mA            0000 0010 <math>\geq</math> 62.5 mA            0000 0011 <math>\geq</math> 93.75 mA            0000 0100 <math>\geq</math> 125 mA            ...            1111 1111 <math>\geq</math> 7.968 A</p>

**Table 208 — Register 0x68**

R68			
Bits	Attribute	Default	Description
7:0	RW	0010 0111	<p>R68 [7:0]: SWD_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node D Output High Current Consumption Warning Threshold</p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '00':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 125 mA            0000 0010 <math>\geq</math> 250 mA            ...            1111 1111 <math>\geq</math> 31.875A</p> <p>If <a href="#">Table 154, Register 0x32</a> [1:0] = '01':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 31.25 mA            0000 0010 <math>\geq</math> 62.5 mA            0000 0011 <math>\geq</math> 93.75 mA            0000 0100 <math>\geq</math> 125 mA            ...            1111 1111 <math>\geq</math> 7.968 A</p>

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

Table 209 — Register 0x69

R69			
Bits	Attribute	Default	Description
7:0	RW	0010 0111	<p>R69 [7:0]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold</p> <p>If Table 154, Register 0x32 [1:0] = '00':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 125 mA            0000 0010 <math>\geq</math> 250 mA            ...            1111 1111 <math>\geq</math> 31.875A</p> <p>If Table 154, Register 0x32 [1:0] = '01':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 31.25 mA            0000 0010 <math>\geq</math> 62.5 mA            0000 0011 <math>\geq</math> 93.75 mA            0000 0100 <math>\geq</math> 125 mA            ...            1111 1111 <math>\geq</math> 7.968 A</p>

Table 210 — Register 0x6A

R6A			
Bits	Attribute	Default	Description
7:0	RW	0010 0000	<p>R6A [7:0]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold</p> <p>If Table 154, Register 0x32 [1:0] = '00':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 125 mA            0000 0010 <math>\geq</math> 250 mA            ...            1111 1111 <math>\geq</math> 31.875A</p> <p>If Table 154, Register 0x32 [1:0] = '01':            0000 0000 = Undefined            0000 0001 <math>\geq</math> 31.25 mA            0000 0010 <math>\geq</math> 62.5 mA            0000 0011 <math>\geq</math> 93.75 mA            0000 0100 <math>\geq</math> 125 mA            ...            1111 1111 <math>\geq</math> 7.968 A</p>

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 211 — Register 0x6D**

R6D			
Bits	Attribute	Default	Description
7:5	RWPE	101	R6D [7:5]: SWA_MAX_VOUT_DETECTION SWA Max Output Voltage Detection Threshold <sup>[1]</sup> 000 = 700 mV 001 = 800 mV ... 111 = 1400 mV
4	ROE	0	R6D [4]: SWA_UNSUPPORTED_VOLTAGE_DETECTION_STATUS SWA Output Voltage Programmed Value Exceed the Threshold Setting Status <sup>[2].[3]</sup> 0 = SWA is programmed less than threshold 1 = SWA is programmed greater than threshold
3:1	RWPE	101	R6D [3:1]: SWD_MAX_VOUT_DETECTION SWD Max Output Voltage Detection Threshold <sup>[1]</sup> 000 = 700 mV 001 = 800 mV ... 111 = 1400 mV
0	ROE	0	R6D [0]: SWD_UNSUPPORTED_VOLTAGE_DETECTION_STATUS SWD Output Voltage Programmed Value Exceed the Threshold Setting Status <sup>[3].[4]</sup> 0 = SWD is programmed less than threshold 1 = SWD is programmed greater than threshold

NOTE 1 The DIMM vendor sets this threshold during the assembly.

NOTE 2 The PMIC checks the SWA output programmed value in [Table 137, Register 0x21, \[7:1\]](#) and [Table 147, Register 0x2B, \[5\]](#) and compares it against the threshold set in [Table 211, Register 0x6D \[7:5\]](#) after PMIC receives VR Enable command (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on). If SWA output programmed value exceeds the threshold, it sets this register to '1'.

NOTE 3 This register can only be cleared after CAMM2 vendor region password is provided and with a command code: R39 = 0x86 only.

NOTE 4 The PMIC checks the SWD output programmed value in [Table 139, Register 0x23, \[7:1\]](#) and [Table 147, Register 0x2B, \[4\]](#) and compares it against the threshold set in [Table 211, Register 0x6D \[3:1\]](#) after PMIC receives VR Enable command (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on). If SWD output programmed value exceeds the threshold, it sets this register to '1'.

## 8.5 CAMM2 Vendor Region Register Definition (cont'd)

**Table 212 — Register 0x6E**

R6E			
Bits	Attribute	Default	Description
7:5	RWPE	001	R6E [7:5]: SWB_MAX_VOUT_DETECTION SWB Max Output Voltage Detection Threshold <sup>[1]</sup> 000 = 700 mV 001 = 800 mV ... 111 = 1400 mV
4	ROE	0	R6E [4]: SWB_UNSUPPORTED_VOLTAGE_DETECTION_STATUS SWB Output Voltage Programmed Value Exceed the Threshold Setting Status <sup>[2],[3]</sup> 0 = SWB is programmed less than threshold 1 = SWB is programmed greater than threshold
3	RV	0	R6E [3]: Reserved
2:1	RWPE	11	R6E [2:1]: SWC_MAX_VOUT_DETECTION SWC Max Output Voltage Detection Threshold <sup>[1]</sup> 00 = 1900 mV 01 = 2000 mV 10 = 2100 mV 11 = 2200 mV
0	ROE	0	R6E [0]: SWC_UNSUPPORTED_VOLTAGE_DETECTION_STATUS SWC Output Voltage Programmed Value Exceed the Threshold Setting Status <sup>[3],[4]</sup> 0 = SWC is programmed less than threshold 1 = SWC is programmed greater than threshold

NOTE 1 The DIMM vendor sets this threshold during the assembly.

NOTE 2 The PMIC checks the SWB output programmed value in [Table 141, Register 0x25, \[7:1\]](#) and [Table 147, Register 0x2B, \[3\]](#) and compares it against the threshold set in [Table 212, Register 0x6E \[7:5\]](#) after PMIC receives VR Enable command (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on). If SWB output programmed value exceeds the threshold, it sets this register to '1'.

NOTE 3 This register can only be cleared after CAMM2 vendor region password is provided and with a command code: R39 = 0x86 only.

NOTE 4 The PMIC checks the SWC output programmed value in [Table 143, Register 0x27, \[7:1\]](#) and [Table 147, Register 0x2B, \[0\]](#) and compares it against the threshold set in [Table 212, Register 0x6E \[2:1\]](#) after PMIC receives VR Enable command (either via VR\_EN pin or I<sup>2</sup>C/I<sup>3</sup>C bus command or auto power on). If SWC output programmed value exceeds the threshold, it sets this register to '1'.

## 9 Package Outline Drawings

### 9.1 Package Mechanical Drawing

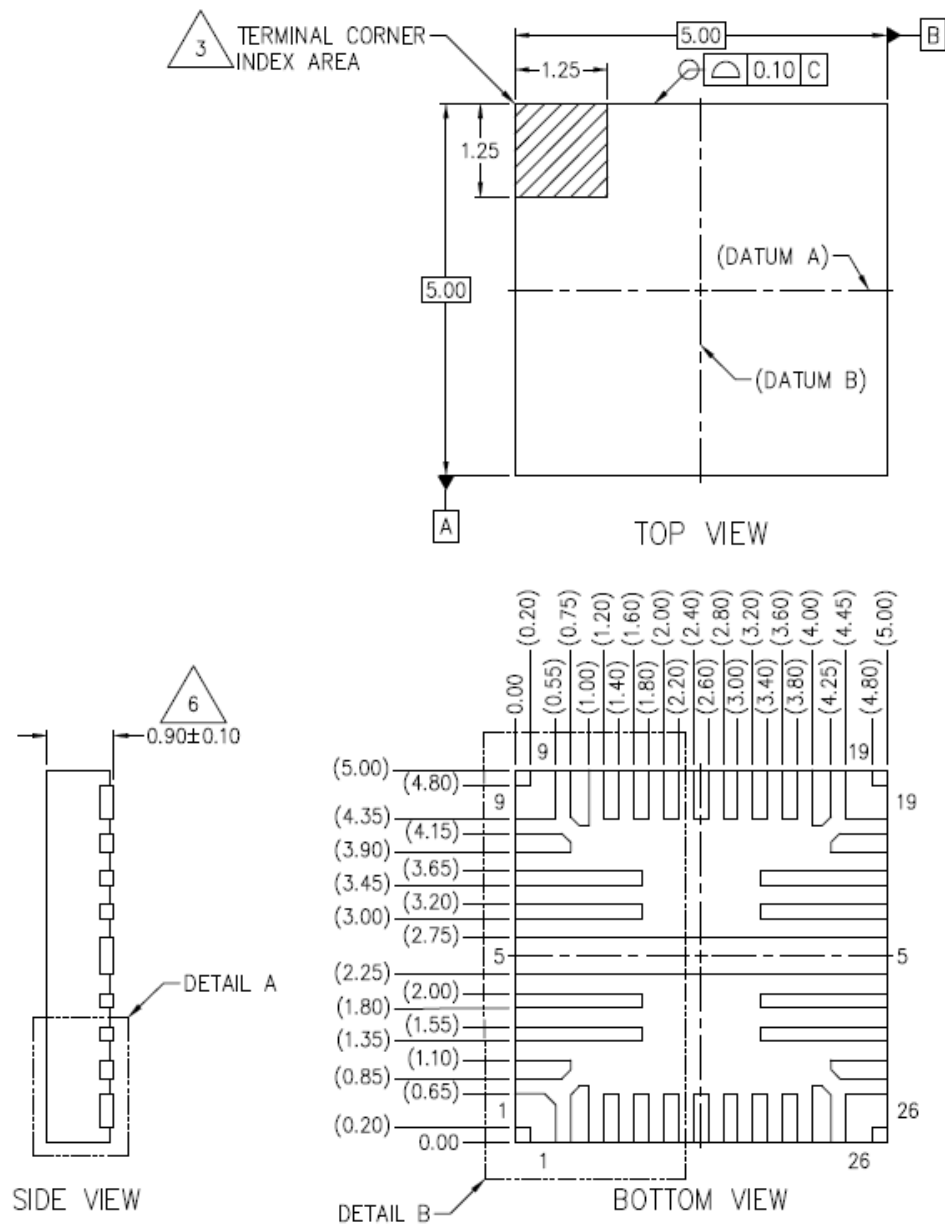
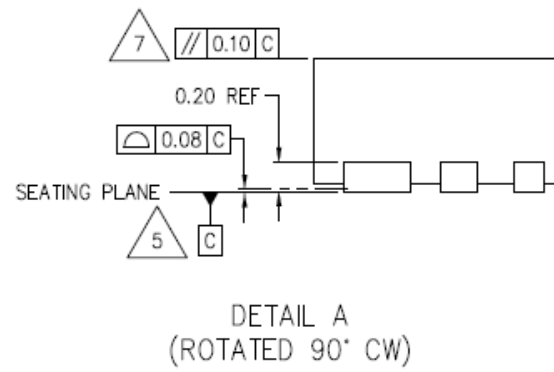


Figure 44 — Package Mechanical Outline

## 9.1 Package Mechanical Drawing (cont'd)



**Figure 45 — Detail A Drawing**

## 9.1 Package Mechanical Drawing (cont'd)

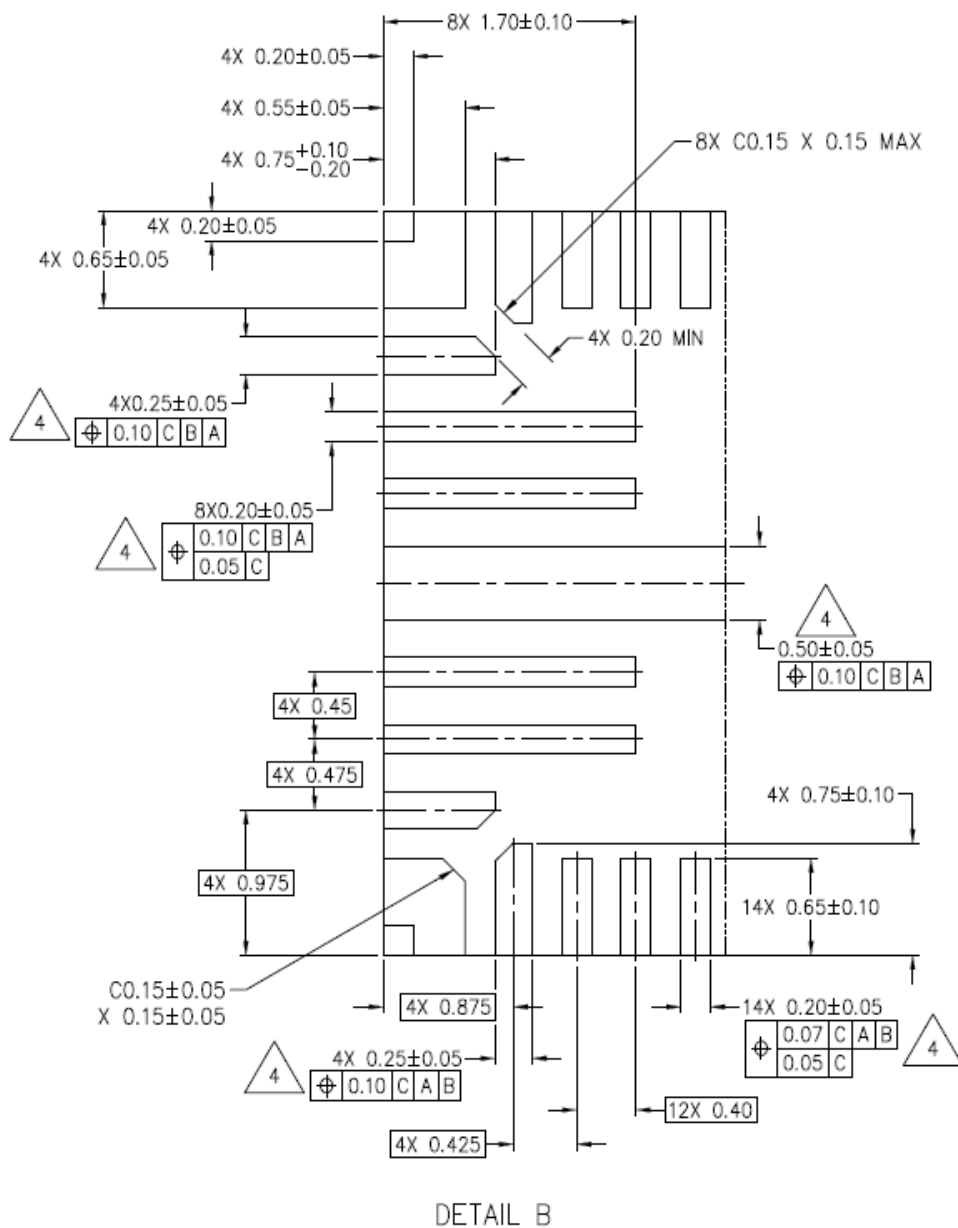


Figure 46 — Detail B Drawing

## 9.1 Package Mechanical Drawing (cont'd)

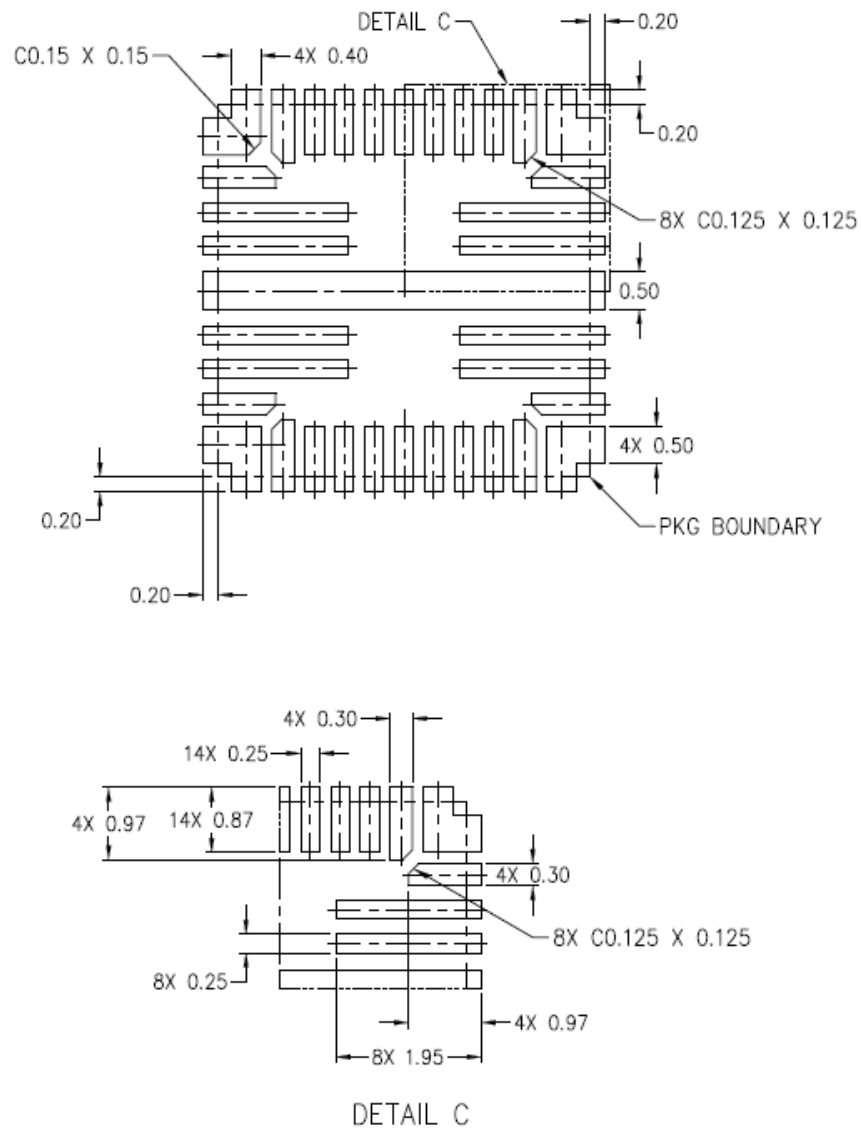


Figure 47 — Reference PCB Land Pattern





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**Standard Improvement Form****JEDEC Standard JESD301-3**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

---

2. Recommendations for correction:


---

3. Other suggestions for document improvement:


---

Submitted by

Name: \_\_\_\_\_

Company: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

Phone: \_\_\_\_\_

E-mail: \_\_\_\_\_

Date: \_\_\_\_\_

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